BAT32A279 Datasheet

Ultra-low power 32-bit microcontroller based on ARM® Cortex-M0®+

Built-in 512K bytes Flash, rich analog functions, timers and various communication interfaces

V1.01

Function

- **Ultra-low power operating environment:**
  - Supply voltage range: 2.0V to 5.5V
  - Temperature range: -40°C to 125°C
  - Low power modes: sleep mode, deep sleep mode
  - Operating power consumption: 100uA/MHz@64MHz
  - Power consumption in deep sleep mode: 1.5uA
  - Deep sleep mode +32.768K + RTC operation: 1.9uA
- **Kernel:**
  - ARM®32-bitCortex®-M0+ CPU
  - Operating frequency: 32KHz to 64MHz
- **Memory:**
  - 512KB Flash memory, program shared with data storage
  - 20KB dedicated data Flash memory
  - 64KB SRAM MEMORY WITH PARITY
- **Power and reset management:**
  - Built-in power-on reset (POL) circuitry
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set).
- **Clock Management:**
  - Built-in high-speed oscillator, accuracy (±1%). 1MHz to 64MHz system clock and peripheral module action clock are available
  - Built-in 15KHz low-speed oscillator
  - Built-in 1 channel PLL
  - Support 1MHz ~ 20MHz external crystal oscillator, support stop vibration monitoring
  - Supports 32.768KHz external crystal oscillator for correction of internal high-speed oscillators
- **Multiplier/Divider Module:**
  - Multiplier: Supports single-cycle 32bit multiplication operations
  - Divider: Supports 32bit signed integer division and requires only 8 CPU clock cycles to complete the operation
- **Enhanced DMA controller:**
  - An interrupt triggers a start.
  - Transmission modes are selectable (normal transfer mode, repeat transfer
- **Input/output port:**
  - I/O ports: 59-93
  - Capable of N-channel open-drain, TTL input buffering, and internal pull-up switching
  - Built-in key interrupt check-out function
  - Control circuitry with built-in clock output/buzzer output
- **Serial two-wire debugger (SWD).**
- **Rich timers:**
  - 16-bit timer: 17 channels (with PWM function and motor dedicated PWM function).
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and support for a wide range of clock correction).
  - Watchdog timer (WWDT): 1
  - SysTick timer
- **Rich and flexible interfaces:**
  - Three serial communication units: serial communication unit 0 can be freely configured as 2-channel standard UART or 4-channel 3-wire SPI or 4-channel simple I^2C; Serial communication unit 1 or 2 can be freely configured as 1-channel standard UART or 2-channel 3-wire SPI or 2-channel simple I^2C; (UART of unit 0 supports LIN Bus communication, SPI00 channel supports 4-wire SPI communication)
  - Standard SPI: 2 channels (supports 8-bit and 16-bit).
  - Standard I^2C: 2 channels
  - CAN: 3 channels
  - LCD BUS interface: support 8080, 6800 connectors
- **Security features:**
  - Complies with IEC/UL 60730 related standards
  - Abnormal storage space access error is

mode, block transfer mode, and chain transfer mode).
- The source/destination field is optional for full address space range

- **Linkage controller:**
  - It can link event signals together to achieve the linkage of peripheral functions.
  - There are 23 types of event inputs and 10 types of event triggers.
- **Rich analog periphery:**
  - 12-bit precision ADC converter with slew rate 1 42Msps, 28 external analog channels, internal optional PGA output as a conversion channel, with temperature sensor, support for single-channel conversion mode and 2, 3, 4-channel scanning conversion mode. Conversion range: 0 to positive reference voltage
  - 8-bit precision D/A converter, 2-channel analog output, real-time output function, output voltage range 0~V_{DD}
  - Comparator (CMP) with built-in two-channel hysteresis comparator, selectable input source, and selectable external or internal reference voltage reference
  - Programmable gain amplifier (PGA) with two channels of PGA to program 4/8/10/12/14/16/32 gains with an external GND pin that can be used as differential mode

reported
- Supports RAM parity
- Supports hardware CRC verification
- Supports critical SFR protection against misoperation
- 128-bit unique ID number
- Flashsecondary protection in debug mode (Level1: only flash full-domain erasure, no read or write; Level2: The emulator connection is invalid and cannot be operated on flash).

- **Package:**
  - Support 64Pin, 80Pin, 100Pin multiple packages

1 Overview

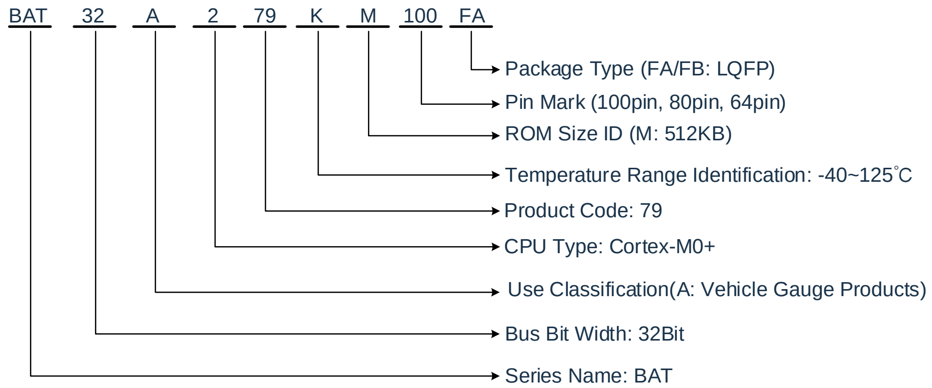
1.1 Brief Introduction

BAT32A279 series conforms to AEC-Q100 automotive product standard, -40~125°C operating ambient temperature, support 64~100Pin in a variety of LQFP packages. This product uses the 32bit of the high-performance ARM®Cortex®-M0+ RISC core, operating up to 64MHz, uses high-speed embedded flash memory (SRAM up to 64 KB, program/data flash up to 512KB). This product integrates a variety of standard interfaces such as I^2C, SPI, UART, LIN, CAN bus and LCD bus interface. Integrated 12bit A/D converter, temperature sensor, 8bit D/A converter, comparator, programmable gain amplifier. The 12bit A/D converter can acquire external sensor signals to reduce system design costs. The 8bit D/A converter can be used for audio playback or power control. An integrated on-chip temperature sensor enables real-time monitoring of the external ambient temperature. The chip's integrated comparator supports both high-speed and low-speed operating modes, control feedback from high-speed motors in high-speed mode, and battery monitoring in low-speed mode. Integrate a variety of advanced timer modules, load 1-channel SysTick timer, 17-channel 16bit timer, 1-channel 15bit interval timer, watchdog timer and real-time clock and other functions, and can support general-purpose PWM and motor dedicated PWM and other applications.

The BAT32A279 also features excellent low-power performance, supporting two low-power modes of sleep and deep sleep, providing design flexibility. It consumes 100uA/MHz @64MHz and consumes only power in deep sleep mode 1.5uA for battery-powered, low-power devices. At the same time, due to the integrated event linkage controller, it can realize the direct connection between hardware modules without CPU intervention, which is faster than using interrupt response. At the same time, the frequency of CPU activity is reduced, which prolongs battery life.

These features make the BAT32A279 microcontroller family superior reliability, rich integrated peripheral functions, and excellent low-power performance, which make them widely applicable to the development of automotive products.

1.2 List of Product Models



BAT32A279 product list:

Number of pins	Package	Product model
64 pins	64-pin plastic LQFP (7X7mm, 0.4mm pitch).	BAT32A279KM64FB
80 pins	80-pin plastic LQFP (12X12mm, 0.5mm pitch).	BAT32A279KM80FA
100 pins	100-pin plastic LQFP (14X14mm, 0.5mm pitch).	BAT32A279KM100FA

FLASH, SRAM capacity:

Flash memory	Specific data Flash memory	SRAM	BAT32A279		
			64 pins	80 pins	100 pins
512KB	20KB	64KB	BAT32A279KM64	BAT32A279KM80	BAT32A279KM100

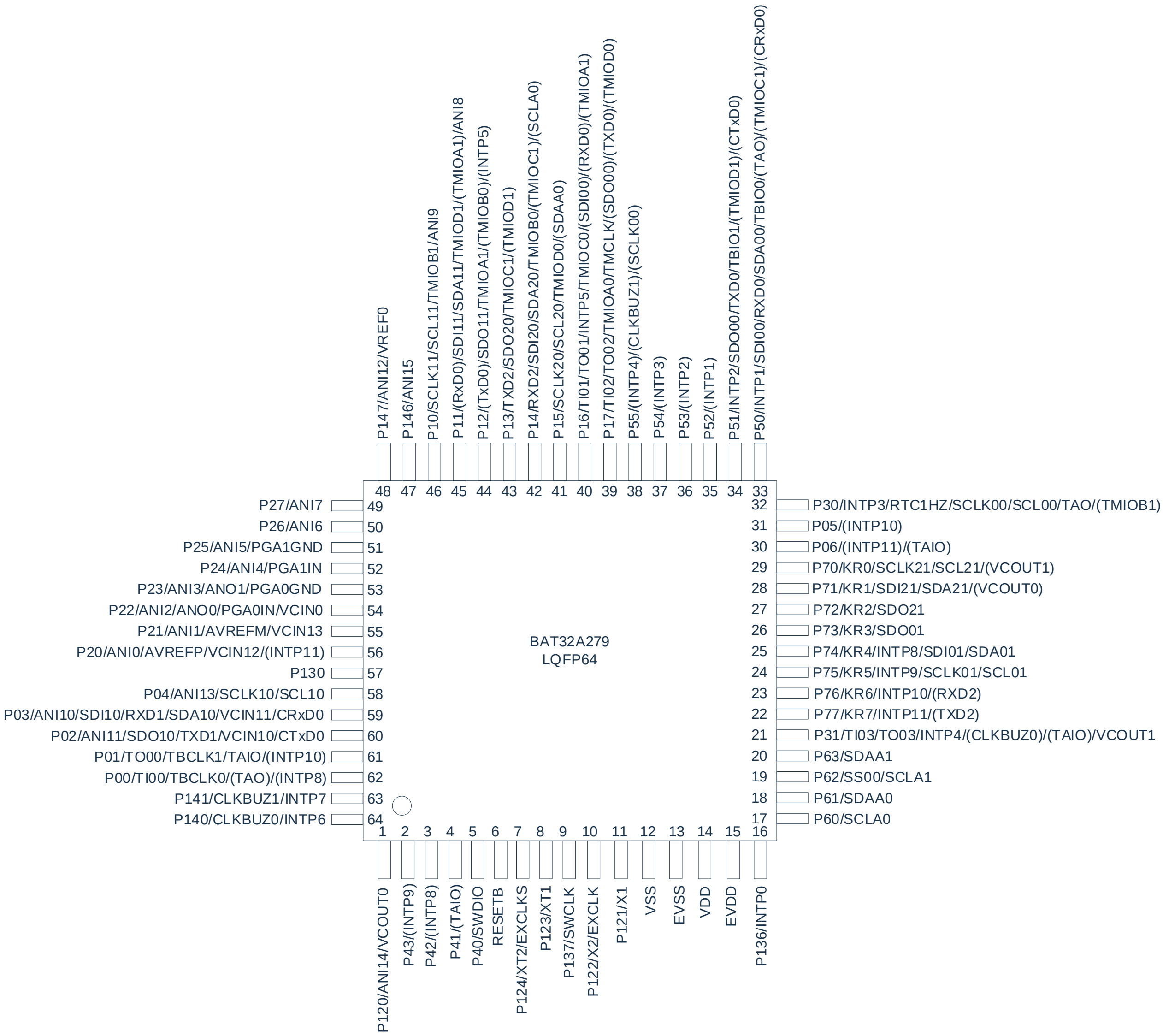
BAT32A279 Product Selection Table:

Part No.	Kernel	Frequency (MHz).	Minimum operating voltage (V).	Maximum operating voltage (V).	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	DMA	GPIO	12bit ADC	8bit DAC	Comparator CMP	Amplifier PGA	Universal timer (16bit).	Real-time clock (RTC).	Watchdog timer (WDT).	Asynchronous serial bus (UART).	Synchronous serial bus (SPI).	IIC bus	LIN bus	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32A279 KM64FB	M0+	64	2.0	5.5	512	64	20	37	59	16+4	2	2	2	17	1	1	3	6	2+6	1	1	Y	Y	LQFP 64
BAT32A279 KM80FA	M0+	64	2.0	5.5	512	64	20	38	75	22+4	2	2	2	17	1	1	4	1+8	2+8	1	2	Y	Y	LQFP 80
BAT32A279 KM100FA	M0+	64	2.0	5.5	512	64	20	40	93	28+4	2	2	2	17	1	1	4	2+8	2+8	1	3	Y	Y	LQFP 100

1.3 Top View

1.3.1 BAT32A279KM64FB

- 64-pin plastic LQFP (7x7mm, 0.4mm pitch).

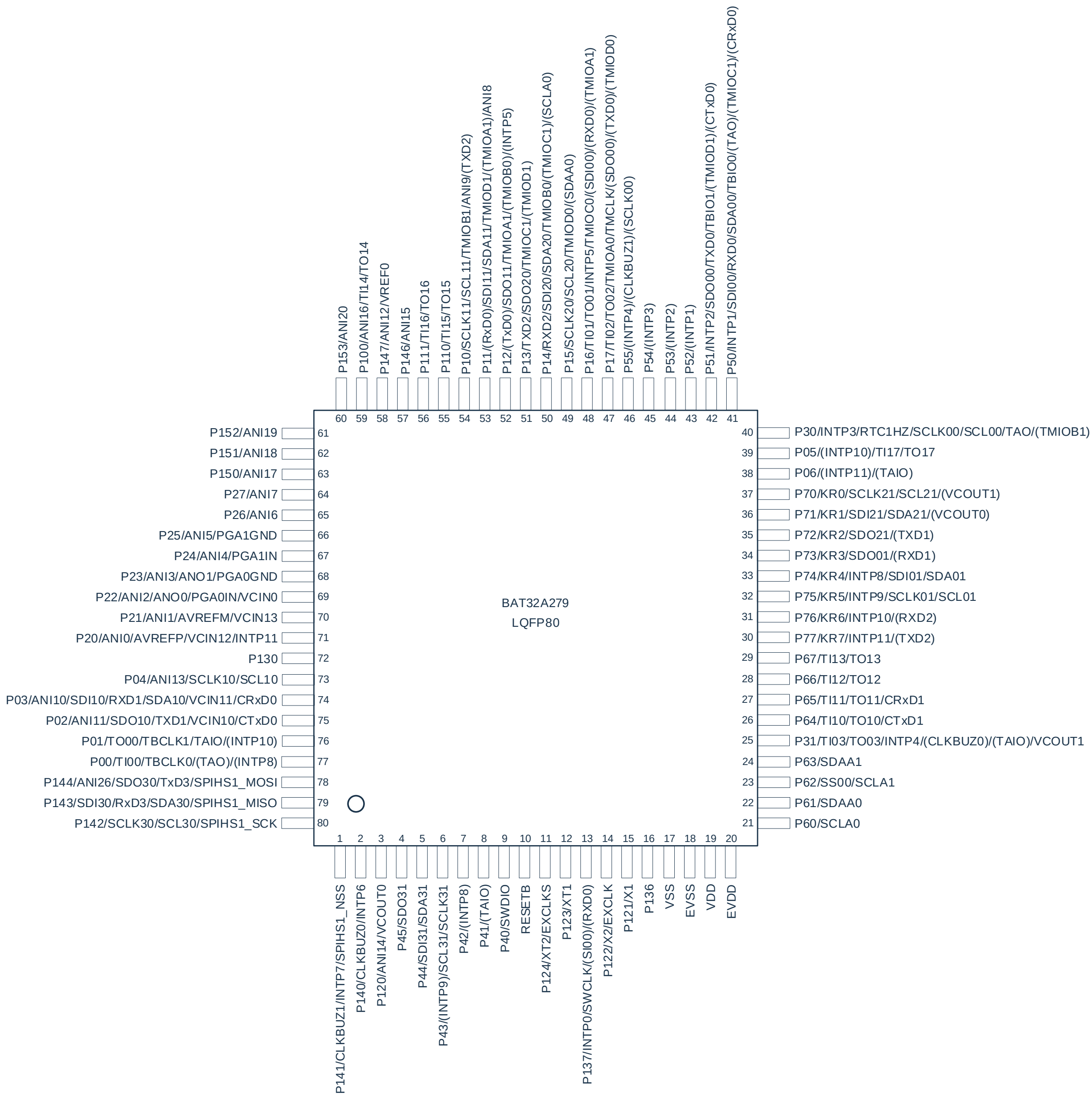


Remark:

1. The EV_{SS} pin and the V_{SS} pin must be the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case of application areas where noise generated from the microcontroller needs to be reduced, it is recommended to supply power to V_{DD} and EV_{DD} separately and to supply V_{SS} and EV_{SS} Noise countermeasures such as individual grounding.
4. The functions in the preceding figure ( ) can be assigned by setting the peripheral I/O redirection registers.

1.3.2 BAT32A279KM80FA

- 80-pin plastic LQFP (12x12mm, 0.5mm pitch).

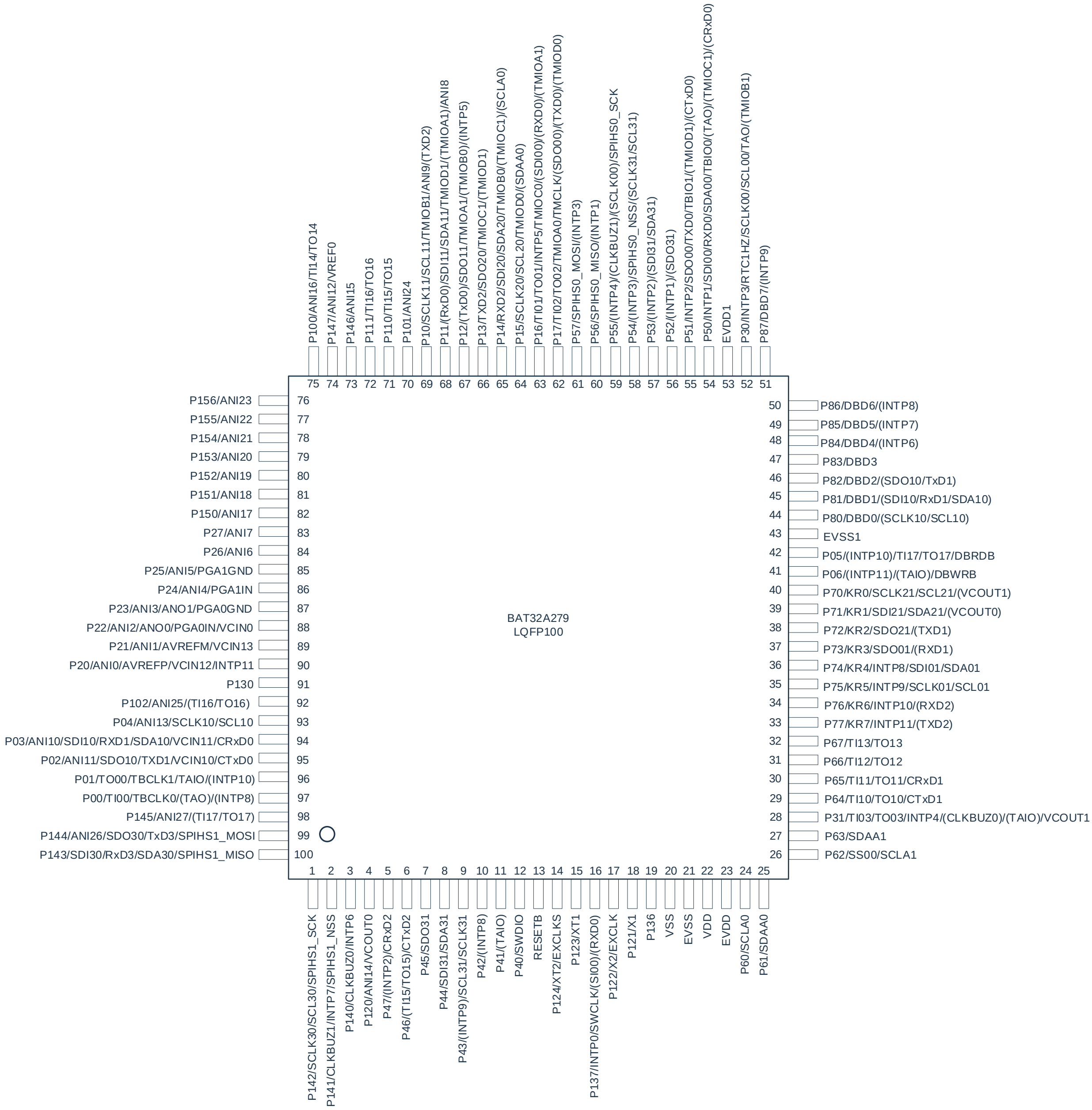


Remark:

1. The EV_{SS} pin and the V_{SS} pin must be the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case of application areas where noise generated from the microcontroller needs to be reduced, it is recommended to supply power to V_{DD} and EV_{DD} separately and to supply V_{SS} and EV_{SS} Noise countermeasures such as individual grounding.
4. The functions in the preceding figure ( ) can be assigned by setting the peripheral I/O redirection registers.

1.3.3 BAT32A279KM100FA

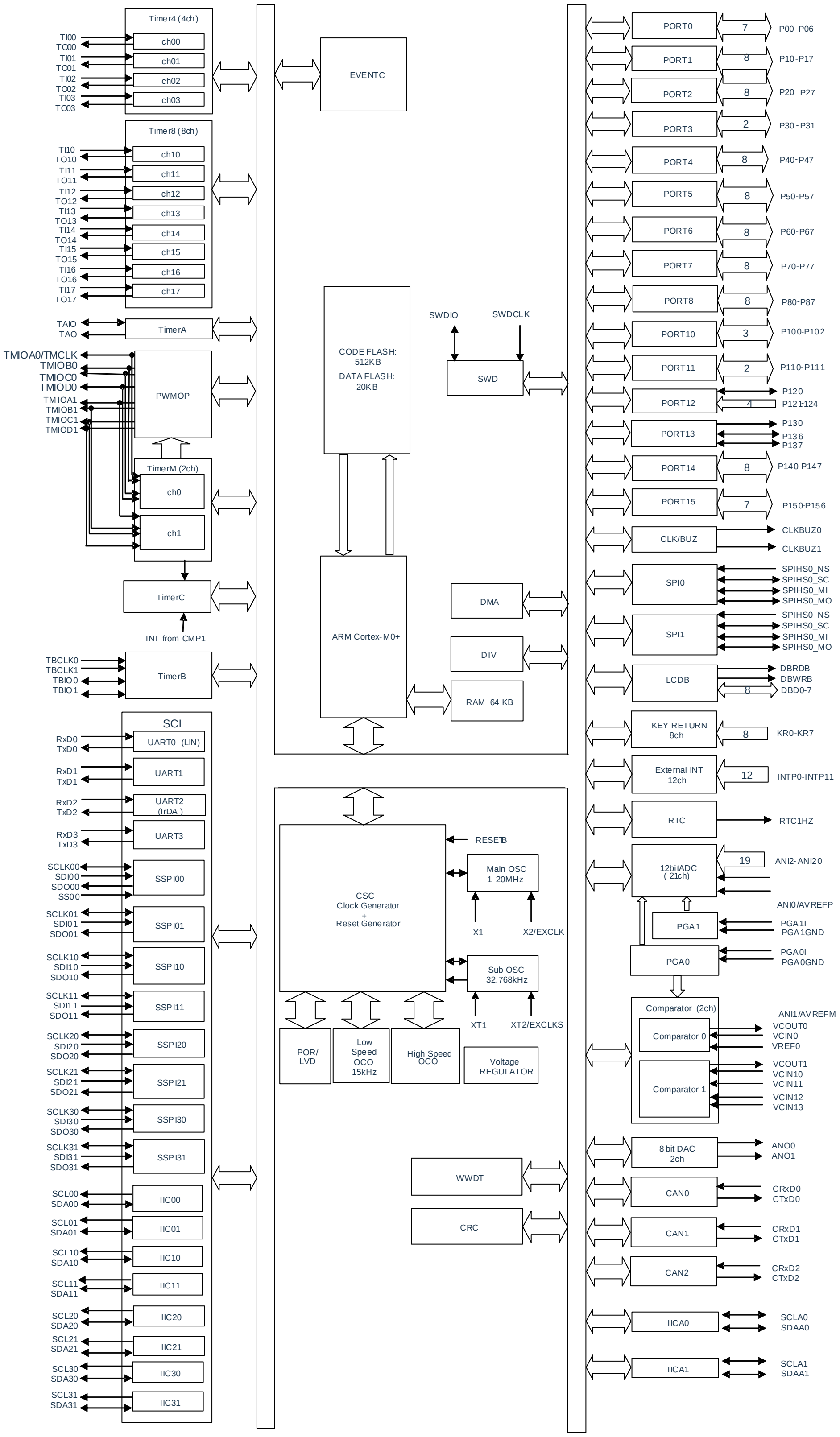
- 100-pin plastic LQFP (14x14mm, 0.5mm pitch).



Remark:

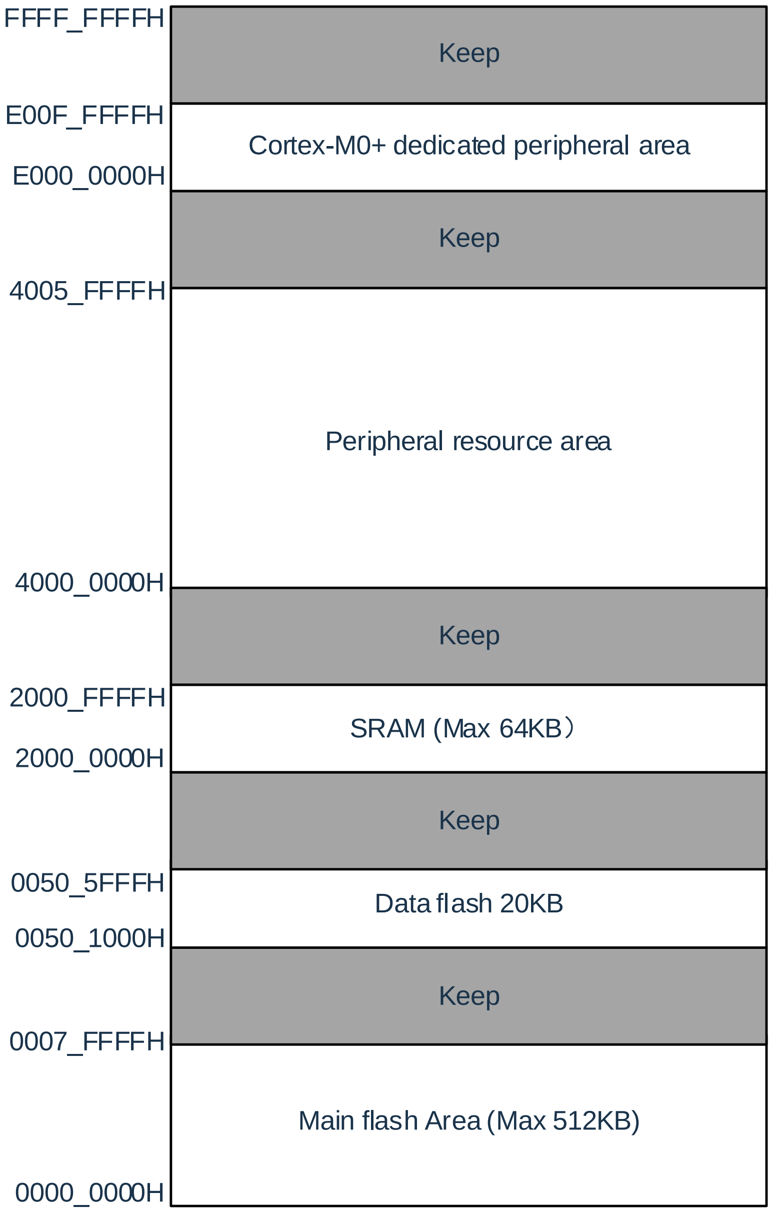
1. The EV_{SS} pin and the V_{SS} pin must be the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case of application areas where noise generated from the microcontroller needs to be reduced, it is recommended to supply power to V_{DD} and EV_{DD} separately and to supply V_{SS} and EV_{SS} Noise countermeasures such as individual grounding.
4. The functions in the preceding figure ( ) can be assigned by setting the peripheral I/O redirection registers.

2 Product Structure Diagram



Note: The above figure is a block diagram of a 100-pin product, and some functions of products below 100 pin are not supported

3 Memory Mapping



4 Pin Function

4.1 Port Functionality

The relationship between the power supply and the pin is shown below.

Power/Ground	The corresponding pin
EV_{DD}/EV_{SS}	• Port pins other than P20~P27, P121~P124, P137 and RESETB
In_{DD}/V_{SS}	• P20~P27, P121~P124, P13 and RESETB

All ports of this product are divided into five types by type, which are type1 to type5, and the corresponding conditions are as follows:

type 1: Bidirectional I/O function

type 2: NOD function, corresponding to pin P60-P63

type 3: Only input functions, such as clocks, correspond to pins P121-P124

type 4: Output function only, corresponding to pin P130

type 5: RESET function, corresponding to pin RESETB

For details of the lead frame diagrams for each type, see 4.3The Port Type.

4.1.1 64 Pin Product Pin Function Description

(1/2)

Function name	Input/output	After the reset is released	Multiplexing function	Description of the feature
P00	Input/output	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P01, P03, and P04 can be set to TTL Input buffering. The outputs of P00 and P02~P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02，P03, P04 can be set as analog inputs.
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)	
P06			(INTP11)/(TAIO)	
P10	Input/output	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13 to P15, and P17 can be set to N-channel open-drain outputs (EVDD withstand voltage). P10 and P11 can be set to analog inputs.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0) /(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(SDO00) /(TXD0)/(TMIOD0)	
P20	Input/output	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input/output port that can be specified as an input or output in bits. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	Input/output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3 A 2-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	

				TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (EVDD withstand voltage).

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Function name	Input/output	After the reset is released	Multiplexing function	Function
P40	Input/output	Input port	SWDIO	Port 4 A 4-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors.
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)	
P50	Input/output	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0 /(TAO)/(TMIOC1)/(CRxD0)	Port 5 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of P50 and P55 can be set to TTL input buffers. The outputs of P50, P51, and P55 can be set to N-channel open-drain outputs (EVDD withstand voltage).
P51			INTP2/SDO00/TXD0/TBIO1 /(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	Input/output	Input port	SCLA0	Port 6 A 4-bit input/output port that can be specified as an input or output in bits. The output of P60~P63 is an N-channel open-drain output (6V withstand voltage).
P61			SDAA0	
P62			SS00	
P63			—	
P70	Input/output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The outputs of P71 and P74 can be programmed to N-channel open-drain outputs (EVDD withstand voltage).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P120	Input/output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/output port and 4-bit input dedicated port Only the P120 can specify inputs or outputs. Only the input port of the P120 can be set by software to use the internal pull-up resistor. The P120 can be set to an analog input.
P121	input	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	output	Output port	—	Port 13 1-bit output dedicated port and 2-bit input/output port, P136 and P137 can be specified as input or output in bits. The input port can be set through the software , using an internal pull-up resistor.
P136	Input/output	Input port	INTP0	
P137			SWCLK	
P140	Input/output	Input port	CLKBUZ0/INTP6	Port 14 A 4-bit input/output port that can be specified as
P141			CLKBUZ1/INTP7	

P146		Analog function	ANI15	an input or output in bits. The input port can be set by software using internal pull-up resistors. P146, P147 can be set to analog input.
P147			ANI12/VREF0	
RESETB	input	—	—	An input pin dedicated to external reset, which must be connected to VDD directly or via a resistor when no external reset is used.

Remark:

1. Set each pin to digital or analog (in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.1.2 80 Pin Product Pin Function Description

(1/3)

Function name	Input/output	Relieve After reset	Multiplexing function	Description of the feature
P00	Input/output	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P01, P03, and P04 can be set to TTL Input buffering. The outputs of P00 and P02~P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02, P03, P04 can be set as analog inputs.
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)/TI17/TO17	
P06			(INTP11)/(TAIO)	
P10	Input/output	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13 to P15, and P17 can be set to N-channel open-drain outputs (EV_{DD} withstand voltage). P10 and P11 can be set to analog inputs.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0) /(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(SDO00) /(TXD0)/(TMIOD0)	
P20	Input/output	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input/output port that can be specified as an input or output in bits. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	Input/output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3 A 2-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to TTL input buffering. The output of
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

				the P30 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).

(2/3)

Function name	Input/output	Relieve After reset	Multiplexing function	Function
P40	Input/output	Input port	SWDIO	Port 4 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. P43 and P44 inputs can be set to TTL input buffers and outputs to N-channel open-drain outputs (EV_{DD} withstand voltage) .
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)/SCLK31/SCL31	
P44			SDA31/SDI31	
P45			SDO31	
P50	Input/output	Input port	INTP1/SDI00/RXD0/SDA00 /TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of P50 and P55 can be set to TTL input buffers. The outputs of P50, P51, and P55 can be set to N-channel open-drain outputs (EV_{DD} withstand voltage).
P51			INTP2/SDO00/TXD0/TBIO1 /(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	Input/output	Input port	SCLA0	Port 6 An 8-bit input/output port that can be specified as an input or output in bits. The output of P60~P63 is an N-channel open-drain output (6V withstand voltage).
P61			SDAA0	
P62			SS00/SCLA1	
P63			SDAA1	
P64			TI10/TO10/CTxD1	
P65			TI11/TO11/CRxD1	
P66			TI12/TO12	
P67			TI13/TO13	
P70	Input/output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The outputs of P71 and P74 can be programmed to N-channel open-drain outputs (EV_{DD} withstand voltage).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P100	Input/output	Analog function	ANI16/TI14/TO14	Port 10 A 1-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors.
P110	Input/output	Input	TI15/TO15	Port 11

P111		port	TI16/TO16	A 2-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors.

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Function name	Input/output	After the reset is released	Multiplexing function	Function
P120	Input/output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/output port and 4-bit input dedicated port Only the P120 can specify inputs or outputs. Only the input port of the P120 can be set by software to use the internal pull-up resistor. The P120 can be set to an analog input.
P121	input	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	output	Output port	—	Port 13 1-bit output dedicated port and 2-bit input/output port, P136 and P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.
P136	Input/output	Input port	INTP0	
P137			SWCLK	
P140	Input/output	Input port	CLKBUZ0/INTP6	Port 14 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of the P142 and P143 can be set to TTL input buffers. The output of the P142, P143, P144 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P146, P147 can be set to analog input.
P141			CLKBUZ1/INTP7	
P142			SCLK30/SCL30	
P143			SDI30/RxD3/SDA30	
P144			SDO30/TxD3	
P146		Analog function	ANI15	
P147			ANI12/VREF0	
P150	Input/output	Analog function	ANI17	Port 15 A 4-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. Can be set to analog input.
P151			ANI18	
P152			ANI19	
P153			ANI20	
RESETB	input	—	—	The input dedicated pin for external reset must be connected to V_{DD} directly or via a resistor when no external reset is used.

Remark:

1. Set each pin to digital or analog (in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.1.3 100 Pin Product Pin Function Description

(1/3)

Function name	Input/output	Relieve After reset	Multiplexing function	Description of the feature
P00	Input/output	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P01, P03, and P04 can be set to TTL Input buffering. The outputs of P00 and P02~P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02, P03, P04 can be set as analog inputs.
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)/TI17/TO17	
P06			(INTP11)/(TAIO)	
P10	Input/output	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs for P10 and P14~P17 can be set to TTL Input buffering. The outputs of P10, P11, P13 to P15, and P17 can be set to N-channel open-drain outputs (EV_{DD} withstand voltage). P10 and P11 can be set to analog inputs.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(SDO00)/(TXD0)/(TMIOD0)	
P20	Input/output	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input/output port that can be specified as an input or output in bits. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	

P26			ANI6	
P27			ANI7	
P30	Input/output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3 A 2-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	

(2/3)

Function name	Input/output	Relieve After reset	Multiplexing function	Function
P40	Input/output	Input port	SWDIO	Port 4 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. P43 and P44 inputs can be set to TTL input buffers and outputs to N-channel open-drain outputs (EV_{DD} withstand voltage) .
P41			(TAIO)	
P42			(INTP8)/(TI14/TO14)	
P43			(INTP9)/SCLK31/SCL31	
P44			SDA31/SDI31	
P45			SDO31	
P46			CTxD2/(TI15/TO15)	
P47			CRxD2/(INTP2)	
P50	Input/output	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO) /(TMIOC1)/(CRxD0)	Port 5 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of P50 and P55 can be set to TTL input slowly Rush. The outputs of P50, P51, and P55 can be set to N-channel open-drain outputs (EV_{DD} withstand voltage).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)/(SDO31)	
P53			(INTP2)/(SDI31/SDA31)	
P54			(INTP3)/(SCLK31/SCL31)/SPIHS0_NSS	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)/SPIHS0_SCK	
P56			SPIHS0_MISO/(INTP1)	
P57			SPIHS0_MOSI/(INTP3)	
P60	Input/output	Input port	SCLA0	Port 6 An 8-bit input/output port that can be specified as an input or output in bits.
P61			SDAA0	
P62			SS00/SCLA1	

P63			SDAA1	The output of P60~P63 is an N-channel open-drain output (6V withstand voltage).
P64			TI10/TO10/CTxD1	
P65			TI11/TO11/CRxD1	
P66			TI12/TO12	
P67			TI13/TO13	
P70	Input/output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The outputs of P71 and P74 can be programmed to N-channel open-drain outputs (EV_{DD} withstand voltage).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	

(3/3)

Function name	Input/output	Relieve After reset	Multiplexing function	Function
P80	Input/output	Input port	(SCLK10/SCL10)/DBD0	Port 8 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of P80 and P81 can be set to TTL input buffers. The outputs of P80, P81, and P82 can be set to N-channel open-drain outputs (EV_{DD} Withstand pressure).
P81			(SDI10/RXD1/SDA10)/DBD1	
P82			(SDO10/TXD1)/DBD2	
P83			DBD3	
P84			(INTP6)/DBD4	
P85			(INTP7)/DBD5	
P86			(INTP8)/DBD6	
P87			(INTP9)/DBD7	
P100	Input/output	Analog function	ANI16/TI14/TO14	Port 10 A 3-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors.
P101			ANI24	
P102			(TI16/TO16)/ANI25	
P110	Input/output	Input port	TI15/TO15/(INTP10)	Port 11 A 2-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors.
P111			TI16/TO16/(INTP11)	
P120	Input/output	Analog function	ANI14/VCOUT0	Port 12 1-bit input/output port and 4-bit input dedicated port Only the P120 can specify inputs or outputs. Only the input port of the P120 can be set by software to use the internal pull-up resistor. The P120 can be set to an analog input.
P121	input	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	output	Output port	—	Port 13 1-bit output dedicated port and 2-bit input/output port, P136 and P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.
P136	Input/output	Input port	INTP0	
P137			SWCLK	
P140	Input/output	Input port	CLKBUZ0/INTP6	Port 14 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using internal pull-up resistors. The inputs of the P142 and P143 can be set to TTL input buffers. The output of the P142, P143, P144 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P145, P146, P147 can be set to analog inputs.
P141			CLKBUZ1/INTP7	
P142			SCLK30/SCL30	
P143			SDI30/RxD3/SDA30	
P144			SDO30/TxD3	
P145		Analog function	(TI17/TO17)/ANI27	
P146			ANI15	
P147			ANI12/VREF0	
P150	Input/output	Analog function	ANI17	Port 15 A 4-bit input/output port that can be specified as an input
P151			ANI18	

P152			ANI19	or output in bits. The input port can be set by software using internal pull-up resistors. Can be set to analog input.
P153			ANI20	
P154			ANI21	
P155			ANI22	
P156			ANI23	
RESETB	input	—	—	The input dedicated pin for external reset must be connected to VDD directly or via a resistor when no external reset is used.

Remark:

1. Set each pin to digital or analog (in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.2 Port Multiplexing Function

(1/2)

The feature name	Input/ output	Function
ANI0~ANI27	input	The analog input of the A/D converter
ANO0, ANO1	output	The output of the D/A converter
INTP0~INTP11	input	External interrupt request input Designation of effective edges: ascending edges, falling edges, rising and falling bilateral edges
VCIN0	input	The analog voltage input for comparator 0
VCIN10, VCIN11, VCIN12, VCIN13	input	The analog voltage/reference input for comparator 1
VREF0	input	The reference input for comparator 0
VCOUT0, VCOUT1	output	Comparator output
PGA0IN, PGA1IN	input	PGA input
PGA0GND, PGA1GND	input	PGA reference input
KR0~KR7	input	The key interrupts the input
CLKBUZ0, CLKBUZ1	output	Clock output/buzzer output
RTC1HZ	output	Correction clock (1Hz) output for the real-time clock
RESETB	input	A active-low system reset input must be connected to VDD directly or via a resistor when no external reset is used.
CRxD0, CRxD1, CRxD2	input	Serial data input for CAN
CTxD0, CTxD1, CTxD2	output	Serial data output for CAN
RxD0~RxD3	input	Serial data input for UART0, UART1, UART2, and UART3 interfaces
TxD0~TxD3	output	Serial data output for UART0, UART1, UART2, and UART3
SCL00, SCL01, SCL10, SCL11 SCL20, SCL21, SCL30, SCL31	output	Serial clock output for serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31	Input/output	Serial data input/output of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21, SCLK30, SCLK31	Input/output	Serial clock input/output for serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21, SDI30, SDI31	input	Serial data input for serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
SS00	input	The chip select input for the serial interface SSPI00
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21, SDO30, SDO31	output	SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, Serial data output for SSPI30 and SSPI31
DBD0~DBD7	Input/output	LCD bus data input/output
DBRDB	output	L-CD bus read enable output
DBWRB	output	LCD bus write enable output
SCLA0, SCLA1	Input/output	Clock input/output of serial interface IICA0 and IICA1
SDAA0, SDAA1	Input/output	Serial data input/output of serial interface IICA0 and IICA1

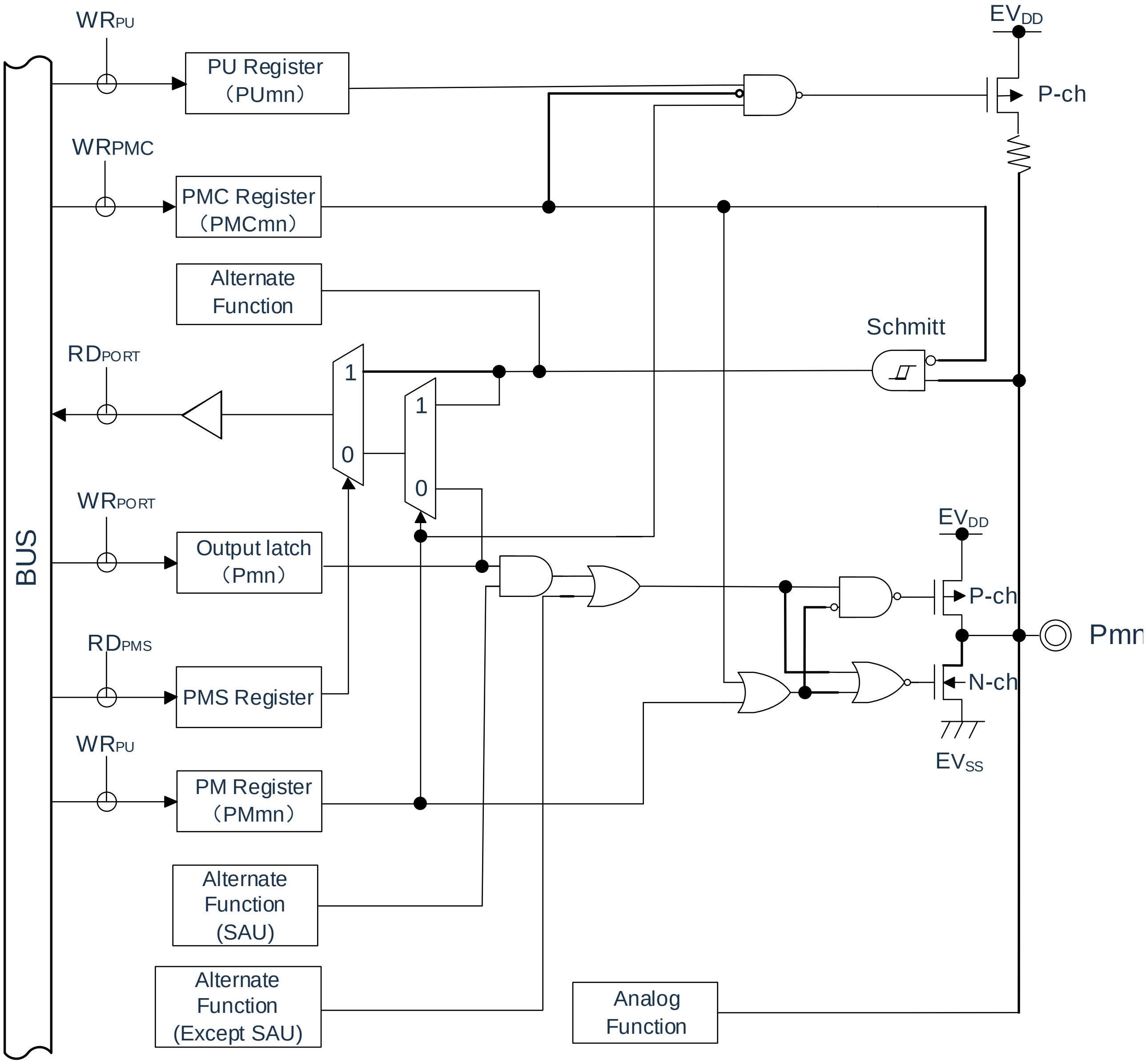
(2/2)

The feature name	Input/output	function
SPIHS0_NSS	input	The chip select input for the serial interface SPIHS0
SPIHS0_SCK	Input/output	Serial clock input/output of serial interface SPIHS0
SPIHS0_MISO	Input/output	Serial data input/output of serial interface SPIHS0
SPIHS0_MOSI	Input/output	Serial data input/output of serial interface SPIHS 0
SPIHS1_NSS	input	Chip select input for the serial interface SPIHS 1
SPIHS1_SCK	Input/output	Serial clock input/output of serial interface SPIHS 1
SPIHS1_MISO	Input/output	Serial data input/output of serial interface SPIHS 1
SPIHS1_MOSI	Input/output	Serial data input/output of serial interface SPIHS 1
TUE00~TI03	input	External counting clock/capture trigger input for 16-bit timer Timer4
TO00~TO03	output	Timer output of the 16-bit timer Timer4
TI10~TI17	input	External count clock/capture trigger input for 16-bit timer Timer8
TO10~TO17	output	Timer output of the 16-bit timer Timer8
TAIO	Input/output	The input/output of Timer TimerA
MAN	output	The output of timer TimerA
TMCLK	input	The external clock input for TimerM for the timer
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	Input/output	Timer TimerM input/output
TBIO0, TBIO1	Input/output	The input/output of timer TimerB
TBCLK0, TBCLK1	input	The external clock input for TimerB for the timer
X1, X2	—	Connect the resonator used for the master system clock.
EXCLK	input	The external clock input to the master system clock
XT1, XT2	—	Connect a resonator for the subsystem clock.
EXCLKS	input	An external clock input to the secondary system clock
In_{DD}	—	＜64, 80Pin product ＞: Power supplies for P20 to P27, P121 to P124, P137, and RESETB pins
EV_{DD}	—	Power supplies for port pins (except P20 to P27, P121 to P124, P137, and RESETB).
AVREFP	input	The positive (+) reference input of the A/D converter
AVREFM	input	The negative (-) reference voltage input for the A/D converter
V_{SS}	—	＜64, 80Pin product ＞: Ground potentials of the P20 to P27, P121 to P124, P137 and RESETB pins
EV_{SS}	—	The ground potential of the port pins (except P20 to P27, P121 to P124, P137, and RESETB).
SWDIO	Input/output	SWD data interface
SWCLK	input	SWD clock interface

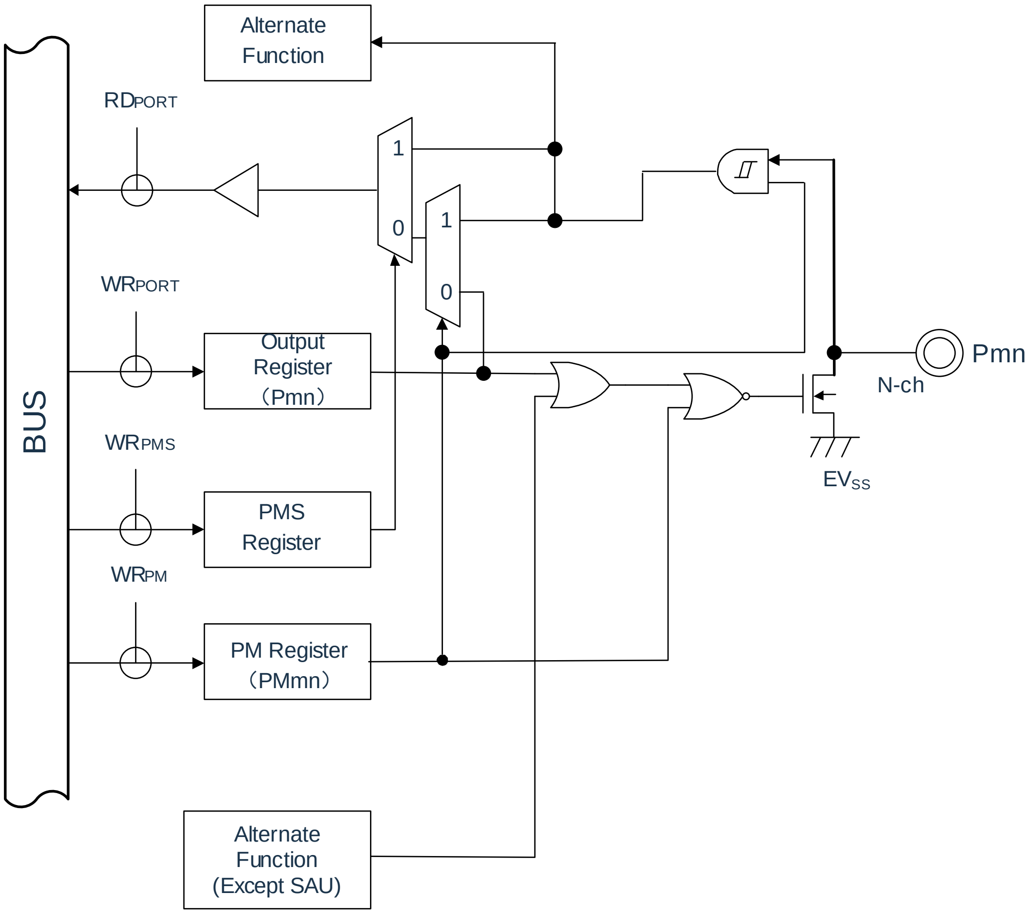
Note: As a countermeasure to noise and lockout, the bypass capacitor must be connected at the shortest distance between V_{DD}-V_{SS}, EV_{DD}-EV_{SS} and with coarse wiring 0.1uF or so).

4.3 The Port Type

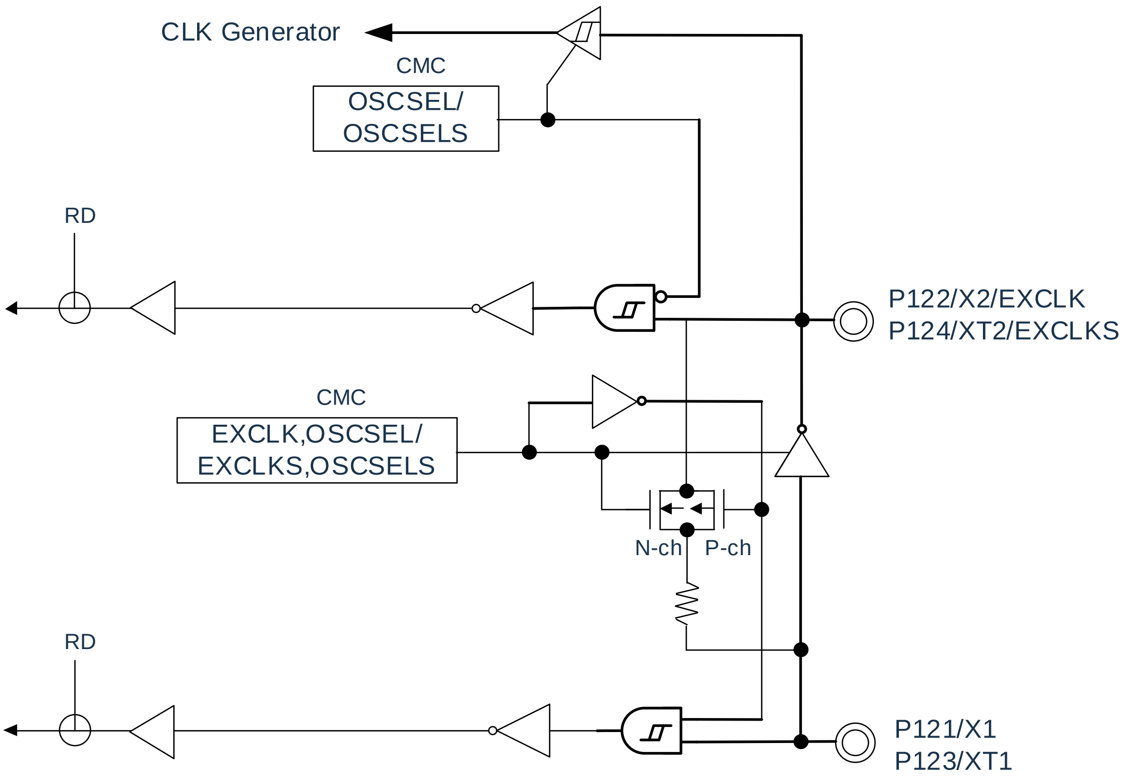
Type 1: Bidirectional I/O capability



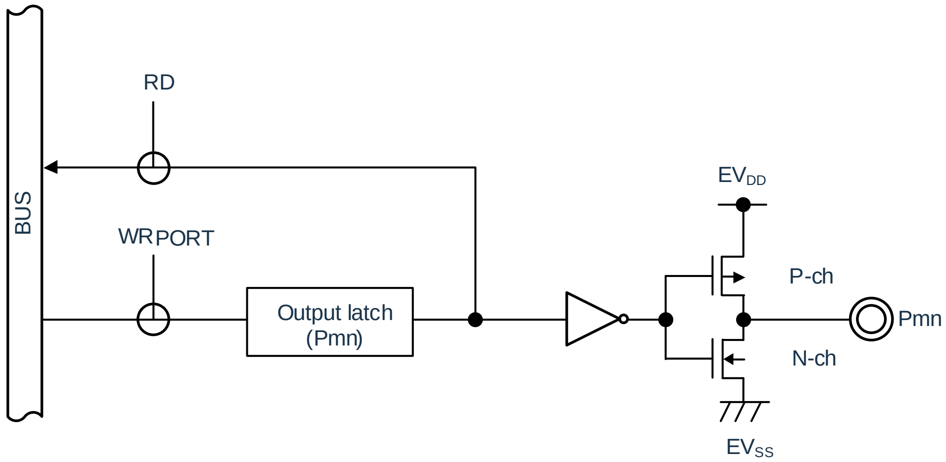
Type 2: NOD functionality



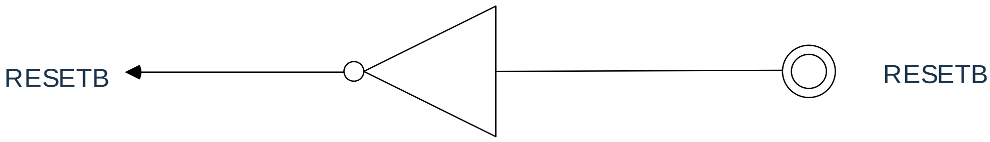
Type 3: Input function only



Type 4: Output function only



Type 5: RESET function



5 Feature Overview

5.1 ARM® Cortex-M0®+ Core

ARM's Cortex-M0+ processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low pin count and low power microcontrollers while providing excellent computing performance and advanced system response to interrupts.

The Cortex-M0+ processor is a 32-bit RISC processor that provides superior code efficiency and delivers the expected high performance of the ARM core Differs from 8-bit and 16-bit devices of the same memory size. The Cortex-M0+) processor has 32 address lines and up to 4G of storage.

The Cortex-M0+ processor in this product integrates the MPU memory protection unit: providing a hardware way to manage and protect memory and control access rights.

The BAT32A279 uses an embedded ARM core and is therefore compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

The BAT32A279 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data share 512K storage space.
- 20KB dedicated data Flash memory.
- Page erasure is supported and the size of each page is 1024byte.
- Supports byte/half-word/word (32bit) programming.

5.2.2 SRAM

The BAT32A279 has a built-in 64K byte embedded SRAM.

5.3 Enhanced DMA Controller

The built-in enhanced DMA (Direct Memory Access) controller enables data transfer between memories without using a CPU.

- Supports activation of DMA via peripheral function interrupts, enabling real-time control through communication, timers, and A/D.
- The source/destination field is optional for the full address space range (when the flash field is the destination address, flash needs to be preset as the programming mode).
- Supports 4 transfer modes (normal transfer mode, repeat transfer mode, block transfer mode, and chain transfer mode).

5.4 Linkage Controller

The linkage controller links the events output by each peripheral function with the peripheral function trigger source. This enables collaborative operation between peripheral functions without using the CPU.

The UMC has the following functions:

- It can link event signals together to achieve the linkage of peripheral functions.
- There are 23 types of event inputs and 10 kinds of event triggers.

5.5 The Clock Generation and Start Up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clock and clock oscillation circuitry.

5.5.1 The Master System Clock

- X1 oscillation circuit: Clock oscillations of 1 to 20 MHz can be generated by connecting resonators to pins (X1 and X2) and can be executed Deep sleep command or set MSTOP to stop oscillation.
- High Speed Internal Oscillator (High Speed OCO): Oscillates by selecting the frequency via option bytes. After the reset is released, the CPU starts running by default with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The maximum frequency is 64Mhz and the accuracy is ± 1.0%.
- An external clock is input from pin (X2) (1 to 20MHz) and can be used by executing a deep sleep command or setting MSTOP The bit sets the input of the external master system clock to be invalid.

5.5.2 Auxiliary System Clock

- XT1 Oscillation Circuit: Generates a clock oscillation of 32.768 KHz from a resonator connected to pins (XT1 and XT2) of 32.768KHz, and can stop the oscillation by setting the XTSTOP bit.
- Input to the external clock by pin (XT2): 32.768KHz, and the input to the external clock can be set to invalidate by setting the XTSTOP bit.

5.5.3 Low-speed Internal Oscillator Clock

- Low-speed internal oscillator (low-speed OCO): Generates a clock oscillation of 15KHz (typical). You cannot use a low-speed internal oscillator clock as a CPU clock. Only the following peripheral hardware can operate through a low-speed internal oscillator clock:
- Watchdog Timer (WWDT)
- Real-Time Clock (RTC)
- 15-bit interval timer
- Timer TimerA

5.5.4 PLL Clock

- PLL: Can be used as a system clock. The PLL can select an external clock from the source clock or an internal high-speed oscillator clock.

5.6 Power Management

5.6.1 Power Supply Mode

V_{DD}: External power supply with a voltage range of 2.0 to 5.5V.
EV_{DD}: External power supply with a voltage range of 2.0 to 5.5V.
The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.

5.6.2 Power-on Reset

The power-on reset circuit (POL) has the following functions.

- An internal reset signal is generated when the power is turned on. If the supply voltage (V_{DD}) is greater than the sense voltage (V_{POL}), the reset is released. However, the reset state must be maintained by voltage detection circuitry or an external reset before the operating voltage range is reached.
- Drag the supply voltage (V_{DD}) and the sense voltage(V_{PDR})Make a comparison, When $V_{DD} < V_{PDR}$, An internal reset signal is generated. But, When the power supply drops, must be less than the operating voltage range, Transfer toDeep sleepmode, or set to reset via voltage detection circuit or external reset. If you want to start running again, you must confirm that the supply voltage has returned to the operating voltage range.

5.6.3 Voltage Detection

The voltage detection circuit sets the operating mode and sense voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Compare the supply voltage (V_{DD}) with the sense voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), An internal reset or interrupt request signal is generated.
- The sense voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by option bytes to select the sense level.
- Runs in deep sleep mode.
- When the power supply rises, the reset state must be maintained by voltage detection circuitry or external reset before reaching the operating voltage range. When the supply drops, it must be transferred to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuitry or an external reset.
- The operating voltage range varies depending on the user option byte setting.

5.7 Low Power Mode

The BAT32A279 supports two low-power modes for the best compromise between low power consumption, short start-up times, and available wake-up sources:

- Sleep Mode: Enters sleep mode by executing sleep commands. Sleep mode is the mode that stops the CPU from running the clock. Each clock continues to oscillate if the high-speed system clock oscillation circuit, high-speed internal oscillator, or subsystem clock oscillation circuit is oscillating before setting sleep mode. Although this mode does not allow the operating current to drop to the level of deep sleep mode, it is an effective mode when you want to restart processing immediately with an interrupt request or if you want to do intermittent operation frequently.
- Deep Sleep Mode: Enter Deep Sleep Mode by executing the Deep Sleep command. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stops the entire system. It can greatly reduce the operating current of the chip. Because deep sleep mode can be lifted by interrupt requests, it can also be run intermittently. However, in the case of the X1 clock, because the wait time to ensure oscillation stability is ensured when the deep sleep mode is released, it is necessary to start processing immediately if you must request an interrupt You must select the sleep mode.

In either mode, the registers, flags, and data memory all remain in the pre-standby mode setting, and also maintain the state of the output latches and output buffers of the input/output ports.

5.8 Reset Function

The following 7 methods generate a reset signal.

1) An external reset is entered via the RESETB pin.
2) An internal reset is generated by a program runaway detection of the watchdog timer.
3) An internal reset is generated by comparing the supply voltage to the sense voltage of the power-on reset (POR) circuit.
4) An internal reset is generated by comparing the supply voltage of the voltage detection circuit (LVD) with the sense voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset.

Internal reset is the same as external reset, and after the reset signal is generated, the program is executed from the addresses written in the addresses 0000H and 0001H.

5.9 Interrupt Function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs, as well as one unmaskable interrupt (NMI) input, as well as multiple internal exceptions.

This product extends 32 maskable interrupt requests (IRQs) and 1 non-maskable interrupt (NMI) to support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

		64 pins	80 pins	100 pins
Interrupts can be masked	external	13	13	13
	internal	33	44	58

5.10 Real-time Clock (RTC).

The real-time clock (RTC) has the following functions:

- Counters with year, month, day, day, hour, minute, and second.
- Fixed-cycle interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month).
- Alarm interrupt function (alarm: week, hour, minute).
- 1Hz pin output function.
- Supports crossover of the secondary system clock or master system clock as the operating clock of the RTC.
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up in deep sleep mode.
- Supports a wide range of clock correction functions.

Year, month, day, hour, minute, and second counts can only be performed if the secondary system clock (32.768KHz) or the crossover of the primary system clock is selected as the operating clock of the RTC. When a low-speed internal oscillator clock (15KHz) is selected, only the fixed-cycle interrupt function can be used.

5.11 Watchdog Timer

1-channel WWDT, 17-bitwatchdog timer runs with option byte setting count. The watchdog timer operates with a low-speed internal oscillator clock (15KHz). A watchdog timer is used to detect a program that is out of control. When a program runaway is detected, an internal reset signal is generated.

The following situations are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When performing a 1-bit operation instruction on the Allow Register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

5.12 SysTick Timer

This timer is dedicated to RTOS, but can also be used as a standard decrement counter.

It features a 24-bit decreasing counter with a self-loading capacity counter that generates a shieldable system interrupt when the self-loading capacity counter reaches 0.

5.13 Timer Timer4

This product contains four 16-bit timer timer unit Timer4. Each 16-bit timer is called a "channel" and can be used as a separate timer or as a combination of multiple channels for advanced timer functionality.

5.13.1 Independent Channel Operation Function

The independent channel operation function is a function that can use any channel independently of other channel operating modes. The stand-alone channel operation function can be used as the following modes:

1) Interval Timer: Can be used as a reference timer for interrupting at fixed intervals (INTTMs).
2) Square Wave Output: Whenever an INTTM interrupt is generated, a flip is triggered to output a square wave of 50% duty cycle from the timer output pin (TO).
3) External Event Counter: Counts the effective edge of the input signal at the timer input pin (TI) and can be used as an event counter to generate an interrupt if a specified number of times are reached.
4) Divider function (Channel 0 of unit 0 only): The input clock of the timer input pin (TI00) is divided and then output from the output pin (TO00).
5) Measurement of input pulse interval: The interval between input pulses is measured by counting at the effective edge of the input pulse signal at the timer input pin (TI) and the effective edge of the next pulse is captured with the count value.
6) Measurement of the high/low width of the input signal: The width of the input signal is measured by counting at one edge of the input signal at the timer input pin (TI) and capturing the count value on the other edge.
7) Delay Counter: The active edge of the input signal at the timer input pin (TI) begins to count and generates an interrupt after any delay period has elapsed.

5.13.2 Multi-channel Linkage Operation Function

The multi-channel linkage operation function can combine the functions implemented by combining the master channel (the reference timer for the main control period) and the slave channel (the timer that operates in accordance with the main control channel). The multi-channel linkage operation function can be used as the following modes:

1) Single-trigger pulse output: Two channels are used in pairs to generate a single-trigger pulse that arbitrarily sets the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: 2 channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: Up to 7 can be generated in fixed periods by extending the PWM function and using 1 master channel and multiple slave channels PWM signal for any duty cycle.

5.13.3 8-bit Timer Operation Function

The 8-bit timer run function uses a 16-bit timer channel as a function for two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.13.4 LIN-bus Support Functionality

Unit Timer4 can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Detection of wake-up signals: The low width is measured by counting the beginning of the falling edge of the input signal at the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the spacer field: After detecting a wake-up signal, the low-level width is measured by counting from the falling edge of the input signal at the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low-level width is greater than or equal to a fixed value, it is considered to be a spacer field.
3) Measurement of synchronous field pulse width: After detecting the interval field, measure the low and high width of the input signal of the UART serial data input pin (RxD). The baud rate is calculated based on the bit interval of the synchronous field measured in this way.

5.14 Timer Timer8

The 80-pin product adds Timer 8, a built-in timer unit containing eight 16-bit timers. Each 16-bit timer is called a "channel" and can be used as a separate timer or as a combination of multiple channels for advanced timer functionality.

5.14.1 Independent Channel Operation Function

The independent channel operation function is a function that can use any channel independently of other channel operating modes. The stand-alone channel operation function can be used as the following modes:

1) Interval Timer: Can be used as a reference timer for interrupting at fixed intervals (INTTM).
2) Square Wave Output: Whenever an INTTM interrupt is generated, a flip is triggered to output a square wave of 50% duty cycle from the timer output pin (TO).
3) External Event Counter: Counts the effective edge of the input signal at the timer input pin (TI) and can be used as an event counter to generate an interrupt if a specified number of times are reached.
4) Measurement of input pulse interval: The interval between input pulses is measured by counting at the effective edge of the input pulse signal at the timer input pin (TI) and the effective edge of the next pulse is captured with the count value.
5) Measurement of the high/low width of the input signal: The width of the input signal is measured by counting at one edge of the input signal at the timer input pin (TI) and capturing the count value on the other edge.
6) Delay Counter: The active edge of the input signal at the timer input pin (TI) begins to count and generates an interrupt after any delay period has elapsed.

5.14.2 Multi-channel Linkage Operation Function

The multi-channel linkage operation function can combine the functions implemented by combining the master channel (the reference timer for the main control period) and the slave channel (the timer that operates in accordance with the main control channel). The multi-channel linkage operation function can be used as the following modes:

1) Single-trigger pulse output: Two channels are used in pairs to generate a single-trigger pulse that arbitrarily sets the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: 2 channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: Up to 7 can be generated in a fixed period by extending the PWM function and using 1 master channel and multiple slave channels PWM signal for any duty cycle.

5.14.3 8-bit timer Operation Function

The 8-bit timer run function uses a 16-bit timer channel as a function for two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.15 Timer TimerA

This product contains a 16bit timer, TimerA, consisting of a reload register and a decrement counter. Available for the following modes of operation:

- Timer mode: Count the count source (the count source can be a clock or an external event)
- Pulse output mode: Counts the counting source and outputs the pulse in case of overflow
- Event Counting Mode: External events are counted and can work in deep sleep mode.
- Pulse Width Measurement Mode: The external pulse width is measured
- Pulse Period Measurement Mode: Measure the external pulse period

5.16 Timer TimerM

This product has a built-in 2-channel 16bit timer TimerM optimized for motor control, which has the following 4 operating modes:

- Timer mode:
  - Input capture function (triggered by an external signal to retrieve the count value to the register).
  - Output comparison function (detects whether the count value and register value are the same, and can change the output of the pin during detection).
  - PWM function (continuous output of arbitrary pulse width)
- Reset synchronous PWM mode: output sawtooth modulation, three-phase waveform without dead time (6pcs)
- Complementary PWM mode: output triangular modulation, three-phase waveform with dead time (6pcs)
- PWM3 Mode: Output Phase PWM Waveform (2pcs)

5.17 Timer TimerB

This product has a built-in 16bit timer TimerB, which has the following 3 modes:

- Timer mode:
  - The input snap function counts on both sides of the rise, fall, or rise/fall edges.
  - Output comparison function "L" level output, "H" level output, or alternate output
- PWM mode: PWM output capable of any duty cycle.
- Phase counting mode: The count value of a 2-phase encoder can be measured automatically.

5.18 Timer TimerC

This product contains a 16bit timer, TimerC, which can be triggered by software, comparator, or timer TimerM for input capture.

5.19 15-bit Interval Timer

A built-in 15-bit interval timer generates an interrupt (INTIT) at any pre-set interval that can be used to wake up from deep sleep mode.

5.20 Clock Output/Buzzer Output Control Circuitry

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is implemented by a dedicated pin.

5.21 Universal Serial Communication Unit

This product has built-in 4 universal serial communication units, each unit has a maximum of 4 serial communication channels. Enables communication functions of standard SPI, Simple SPI, UART, and Simple I^{2}C. Taking the 80pin product as an example, the function allocation of each channel is as follows:

5.21.1 3-Wire Serial Interface (Simple SPI)

The serial clock (SCK) output of the master device transmits and receives data synchronously.

This uses 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI) for a total of 3 A clock-synchronous communication interface for communication lines to communicate.

[Send and receive data].

- 7-16 bits of data length
- Phase control of sending and receiving data
- MSB/LSB preferred choice

[Clock Control].

- The choice of master or slave
- Phase control of the input/output clock
- The transfer period generated by the prescaler and the in-channel counter
- Maximum transfer rate
  Master communication: Max. $F_{CLK}/2$
  Slave communication: Max. $F_{MCK}/6$

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt

[Error detection flag].

- Overflow error

5.21.2 SPI with Slave Chip Select

SPI serial communication interface supporting slave chip select input. This uses a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) together Clock-synchronous communication interface for communication of 4 communication lines.

[Send and receive data].

- 7-16 bits of data length
- Phase control of sending and receiving data
- MSB/LSB preferred choice
- Level settings for sending and receiving data

[Clock Control].

- Phase control of the input/output clock
- The transfer period generated by the prescaler and the in-channel counter
- Maximum transfer rate

  Slave communication: Maximum $F_{MCK}/6$

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt

[Error detection flag].

- Overflow error

5.21.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data receiving (RxD). Using these two communication lines, data is sent and received asynchronously (using the internal baud rate) with other communicating parties in a data frame (consisting of a start bit, data, parity bit, and stop bit). Full-duplex UART communication can be achieved by using two channels dedicated to transmit (even channels) and receive private (odd channels), and can also be achieved by combining Timer4 units and external interrupts (INTP0) to support LIN-bus.

[Send and receive data].

- 7-bit, 8-bit, 9-bit, and 1-6-bit data length
- MSB/LSB preferred choice
- Level setting and inversion selection of transmitted and received data
- Additional parity functions for parity bits
- Attaching of stop bits, detection of stop bits

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt
- Error interrupts caused by frame errors, parity errors, or overflow errors

[Error detection flag].

- Frame error, parity error, overflow error

[LIN-bus function].

- Detection of wake-up signals
- Detection of spaced field (BF).
- Measurement of the synchronous field, calculation of the baud rate

5.21.4 Simple I²C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I²C is designed for single communication with devices such as flash memory and A/D converters, it can only be used as a master device. The start and stop conditions, like the operating control registers, must comply with the AC characteristics and be handled by software.

[Send and receive data].

- Main control transmission, master receiving (limited to single main control master function)
- ACK output function, ACK detection function
- 8 bits of data length (when sending the address, specify the address with a height of 7 bits, and use the lowest bit for R/W control).
- Start and stop conditions are generated through software

[Interrupt function].

- The end of the transfer is interrupted

[Error detection flag].

- ACK error, overflow error

[Features not supported by Simple I²C].

- Slave send, slave receive
- Multi-master function (arbitration failure detection function)
- Wait for the detection function

5.22 Standard Serial Interface SPI

The serial interface SPI has the following two modes:

- Stop-Run mode: This is a mode used when no serial transfer is taking place, which reduces power consumption
- 3-wire serial I/O mode: This mode passes through 3 wires of the serial clock (SCK) and serial data bus (MISO and MOSI). 8-bit or 16-bit data transfer with multiple devices.

5.23 Standard Serial Interface IICA

Serial interface IICA has the following 3 modes:

- Stop-Run mode: This is a mode used when no serial transfer is taking place, which reduces power consumption.
- I^2C-bus mode (multi-master supported): This mode is performed with multiple devices via 2 wires of the serial clock (SCLA) and the serial data bus (SDAA). Bit data transfer. In accordance with the I^2C-bus format, the master device can generate a "start condition" for the slave device on the serial data bus Address, Indication of Transmission Direction, Data, and Stop Condition". The slave automatically detects the received status and data through the hardware. This feature simplifies the I^2C-bus control portion of the application. Because the SCLA and SDAA pins of the serial interface IICA are used as open-drain outputs, the serial clock line and serial data bus require pull-up resistors.
- Wake-up mode: In deep sleep mode, deep sleep mode can be released by generating an interrupt request signal (INTIICA) when receiving the extension code or local station address of the autonomous control device. This is set via the IICA control register.

5.24 Controller CAN

This product can support up to three universal CAN bus interfaces.

5.25 LCD BUS Interface

The LCD bus interface has the following functions:

- Two different bus standards are supported: 8080 mode, 6800 mode
- Supports 8-bit/16-bit read and write operations
- Controllable transmission speed (up to 10MHz)
- DMA transfers can be triggered when internal data transfer is enabled or external bus access is complete
- Supports DMA read and write

5.26 Analog-to-digital Converters (ADC)

This product contains a 12-bit resolution analog-to-digital converter SARADC that converts analog inputs to digital values and supports ADCs up to 21 channels Analog input (ANI0~ANI20). The ADC contains the following features:

- 12-bit resolution, slew rate 142Msps.
- Trigger mode: Support software trigger, hardware trigger and hardware trigger in standby
- Channel selection: Supports two modes: single-channel selection and multi-channel scanning
- Conversion mode: Supports single conversion and continuous conversion
- Operating voltage: Supports operating voltage range of 2.0V⩽ V_{DD}⩽ 5.5V
- Senses the built-in reference voltage (1.45V) and temperature sensor.

The ADC can set various A/D conversion modes using the combination of modes described below.

Trigger mode	Software triggered	Start the conversion with software operation.
	Hardware triggers no-wait mode	Start the conversion by detecting a hardware trigger.
	The hardware triggers the wait mode	In power-off transition standby, power is plugged in by detecting a hardware trigger and the transition automatically begins after the A/D power stabilization wait time.
Channel selection mode	Select the mode	Select 1 channel of analog inputs for A/D conversion.
	Scan mode	A/D conversion of analog inputs for 4 channels sequentially. Four consecutive channels from ANI0 to ANI15 can be selected as analog inputs.
Conversion mode	Single conversion mode	Performs 1 A/D conversion on the selected channel.
	Continuous conversion mode	Continuous A/D conversion of the selected channel until stopped by the software.
Sample time/conversion time	Number of sample clocks/conversion clocks	The sample time can be set by registers, with the default number of sample clocks being 13.5 clk and the minimum number of conversion clocks being 31.5 clk.

5.27 Digital-to-analog Converters (DAC)

This product contains a 2-channel 8-bit resolution analog-to-digital converter DAC that converts digital inputs to analog signals. Has the following characteristics:

- 8-bit resolution D/A converter
- Supports the outputs of two independent analog channels
- R-2R ladder network
- Built-in real-time output function

5.28 Programmable Gain Amplifier (PGA)

Two programmable gain amplifiers (PGA0 and PGA1) are included in this product with the following functions

- There are 7 options for amplification gain per PGA: 4x, 8x, 10x, 12x, 14x, 16x, 32x
- An external pin can be selected as ground for the PGA negative feedback resistor (available as differential mode).
- The output of PGA0 can be selected as an analog input for an A/D converter or as an analog input at the positive end of Comparator 0 (CMP0).
- The output of PGA1 can be selected as an analog input for A/D converters

5.29 Comparators (CMP)

This product has built-in two-channel comparators CMP 0 and CMP1 with the following functions:

- External input and reference multi-channel options for C MP1.
- An external reference input and an internal reference voltage can be selected for the reference.
- The cancellation width of the noise cancellation digital filter can be selected.
- Detects the active edge of the comparator output and generates an interrupt signal.
- Detects the active edge of the comparator output and outputs the event signal to the linkage controller.

5.30 Two-wire Serial Debug Port (SW-DP).

ARM's SW-DP interface allows connection to a microcontroller via a serial line debugging tool.

5.31 Security Features

5.31.1 Flash CRC Computing Functions (High-speed CRC, General-purpose CRC).

Detect data errors in flash memory by CRC operation.

The following two CRCs can be used according to different uses and conditions of use.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash memory area at high speed.
- Generic CRC: In CPU operation, it is not limited to the flash memory area of the code but can be used for multi-purpose inspection.

5.31.2 RAM Parity Error Detection Function

When reading RAM data, parity errors are detected.

5.31.3 SFR Protection Features

Prevent important SFR (Special Function Register) from being overwritten due to CPU runaways.

5.31.4 Illegal Memory Access Detection Function

Detects illegal access to illegal memory areas (areas without memory or areas with restricted access).

5.31.5 Frequency Detection Function

Self-test CPU or peripheral hardware clock frequency using Timer4 units.

5.31.6 A/D Testing Capabilities

The A/D is converted to the A/D converter's positive (+) reference, negative (-) reference, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage the converter performs self-test.

5.31.7 Digital Output Signal Level Detection Function for Input/Output Ports

When the input/ output ports are in output mode, the output level of the pin can be read.

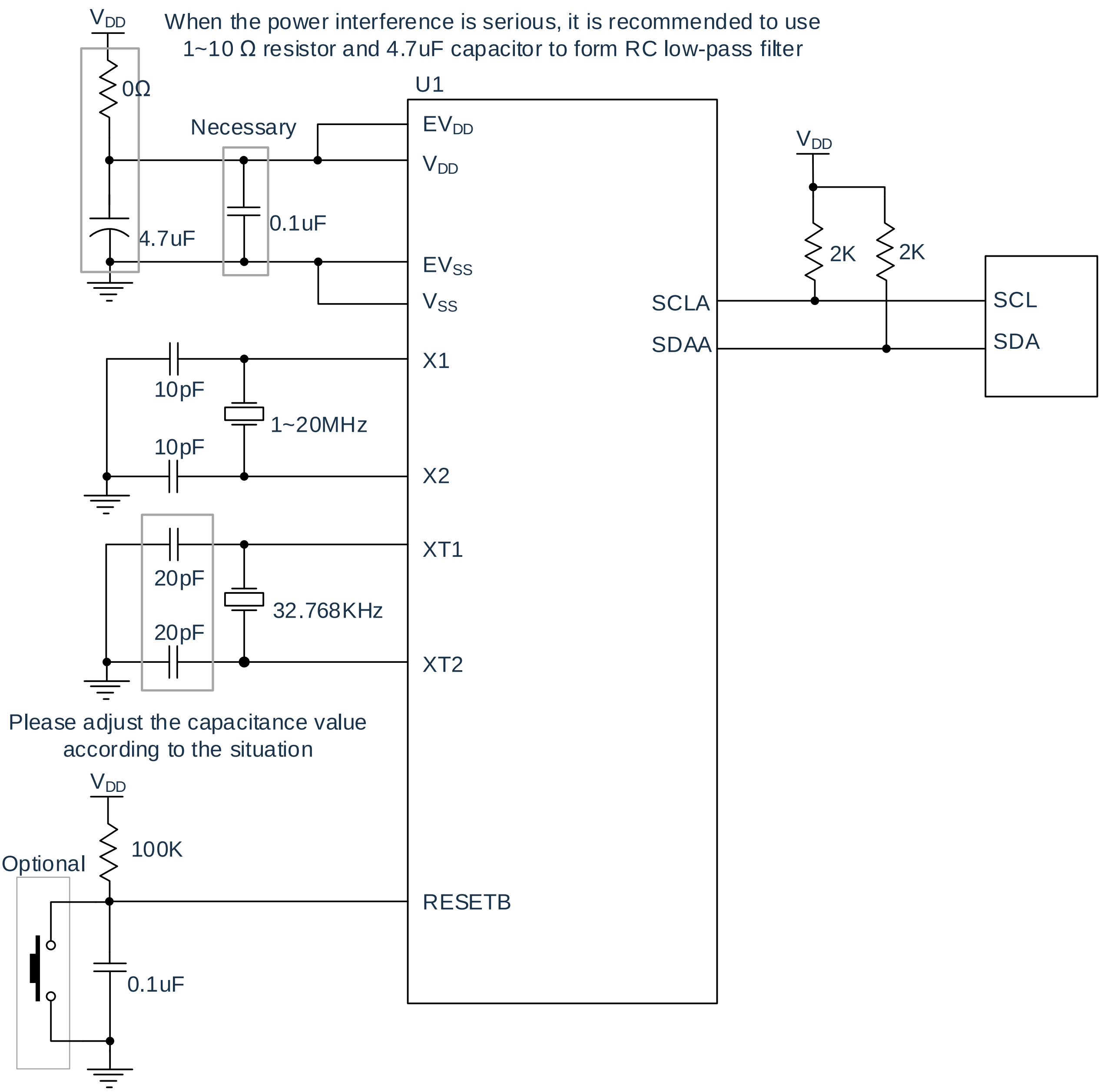
5.32 Key Function

A key interrupt (INTKR) can be generated by pressing the key interrupt input pin (KR0 to KR7) to enter the falling edge.

6 Electrical Characteristics

6.1 Typical Application of Peripheral Circuits

Device connections for typical MCU application peripheral circuits refer to the following:



6.2 Absolute Maximum Voltage Rating

(T_A= -40~125°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.5~6.5	V
	EV_{DD}	-	-0.5~6.5	V
Input voltage	V_{I1}	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P64~P67 P70~P77, P80~P87 P100~P102, P110~P111, P120 P130, P136, P140~P147 P150~P157	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note 1	V
	V_{I2}	P60~P63(N-channel drain open)	-0.3~6.5	V
	V_{I3}	P20~P27, P121~P124, P137 EXCLK, EXCLKS, RESETB	-0.3~V_{DD}+0.3 Note1	V
Output voltage	V_{O1}	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P60~P67 P70~P77, P80~P87 P100~P102, P110~P111, P120 P130, P136, P140~P147 P150~P157	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note1	V
	V_{O2}	P20~P27, P137	-0.3~V_{DD}+0.3 Note1	V
Analog input voltage	V_{AI1}	ANI8~ANI20	-0.3~EV_{DD}+0.3 and -0.3~AV_{REF} (+) +0.3 Note1, 2	V
	V_{AI2}	ANI0~ANI7	-0.3~V_{DD}+0.3 and -0.3~AV_{REF} (+) +0.3 Note1, 2	V

Note1: Not more than 6.5V.

Note2: The pins of the A/D conversion object cannot exceed AV_{REF}(+)+0.3.

Note: Even if 1 item in each project exceeds the absolute maximum rating instantaneously, the quality of the product may be reduced. The absolute maximum rating is the rating that may cause physical damage to the product and must be used in a state that does not exceed the rated value.

Remark:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. AV_{REF}(+): The positive (+) reference voltage of an A/D converter.
3. Use V_{SS} as the reference voltage.

6.3 Absolute Maximum Current Rating

(T_A= -40~125˚C)

Item	Symbol	Condition		Rating	Unit
High output current	I_{OH1}	Each pin	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P64~P67 P70~P77, P80~P87, P100~P102 P110~P111, P120, P130, P136, P137 P140~P147, P150~P157	-40	mA
		Total pins -170mA	P00~P04, P40~P45, P120, P130, P136 P137, P140~P144, P150~P153	-70	mA
			P05, P06, P10~P17, P30, P31 P50~P55, P64~P67, P70~P77, P100 P110~P111, P146, P147	-100	mA
	I_{OH2}	Each pin	P20~P27	-3	mA
		Total pins		-15	mA
Low output current	I_{OL1}	Each pin	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P60~P67 P70~P77, P80~P87, P100~P102 P110~P111, P120, P130, P136, P137 P140~P147, P150~P157	40	mA
		The total pins are 170mA	P00~P04, P40~P45, P120, P130, P136 P137, P140~P144, P150~P153	100	mA
			P05, P06, P10~P17, P30, P31 P50~P55, P60~P67, P70~P77, P100 P110~P111, P146, P147	120	mA
	I_{OL2}	Each pin	P20~P27	15	mA
		Total pins		45	mA
Operating ambient temperature	T_A	Usually run		-40~125	˚C
		When flash programming			
Storage temperature	T_{stg}	-		-65~150	˚C

Note: Even if 1 item in each project exceeds the absolute maximum rating instantaneously, the quality of the product may be reduced. The absolute maximum rating is the rating that may cause physical damage to the product and must be used in a state that does not exceed the rated value.

Remark: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

6.4 Oscillation Circuit Characteristics

6.4.1 X 1, XT1 Features

(T_A= -40~125°C, 2.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonators	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (F_X).	Ceramic resonator/crystal resonator	-	1.0	--	20.0	MHz
X1 clock oscillation settling time	Ceramic resonator/crystal resonator	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic resonator/crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT}).	Crystal resonators	-	32	32.768	35	KHz
XT1 clock oscillation settling time	Crystal resonators	32.768KHz, C=20pF	-	2	-	s

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and refer to the AC characteristics for the execution time of the instruction.
2. Please commission a resonator manufacturer to evaluate the installation circuit and use it after confirming the oscillation characteristics.

6.4.2 Internal Oscillator Features

(T_A= -40~125°C, 2.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonators	Condition	Min	Typ	Max	Unit
Clock Frequency (F_{IH}) of the High-Speed Internal Oscillator Note1,2	-	1.0	-	64.0	MHz
High-speed internal oscillator settling time (T_{SU})	-	-	12	-	us
Clock frequency accuracy of a high-speed internal oscillator	T_A =10~70°C	-1.0	-	+1.0	%
	T_A = 0~105°C	-1.5	-	+1.5	%
	T_A = -10~125°C	-2.0	-	+2.0	%
	T_A = -40~125°C	-4.0	-	+4.0	%
The clock frequency (F_{IL}) of the low-speed internal oscillator	-	12	15	18	KHz

Note 1: Select the frequency of the high-speed internal oscillator via the option byte.

Note 2: Only the characteristics of the oscillation circuit are indicated, please refer to the AC characteristics for the execution time of the instruction.

Remark: The low temperature specification value is guaranteed by the design, and low temperature conditions may occur in mass production.

6.4.3 PLL Oscillator Characteristics

(T_A= -40~125°C, 2.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonators	Condition	Min	Typ	Max	Unit
PLL input frequency [Note1]	-	4.0	-	8.0	MHz
PLL lock time	-	40	-	-	us

Note 1: Only the characteristics of the oscillation circuit are indicated, please refer to the AC characteristics for the command execution time.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level output Current [Note1]	I_{OH1}	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P64~P67 P70~P77, P80~P87, P100~P102 P110~P111, P120, P130, P136 P137, P140~P147, P150~P157 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85°C	-	-	-12.0 [Note2]	mA
			2.0V≤EV_{DD}≤5.5V 85~125°C	-	-	--6.0 [Note2]	
		P00~P04, P40~P45, P120, P130 P136, P137, P140~P144 P150~P157 Total pins (at duty cycle≤70% [Note3])	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	-60.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-12.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-6.0	mA
		P05, P06, P10~P17, P30, P31 P50~P55, P64~P67, P70~P77 P100, P110~P111, P146, P147 pin total (at duty cycle≤70% [Note3]).	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	-80.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-20.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-10.0	mA
		Total pins (at duty cycle≤70% [Note3])	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	-140.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	-60.0	
			2.4V≤EV_{DD}≤4.0V			-30.0	
			2.0V≤EV_{DD}≤2.4V			-15.0	
	I_{OH2}	P20 to P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	-2.5 [Note2]	mA
		Total pins (at duty cycle≤70% [Note3])	2.0V≤V_{DD}≤5.5V	-	-	-10	mA

Note1: This is the current value at which the device is guaranteed to operate even if current flows from the EV_{DD} and V_{DD} pins to the output pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the "duty cycle ≤70% condition". The output current value of 70% of the duty cycle ＞ can be calculated using the following calculation (if the duty cycle is changed to n%).

Total output current of pins = (I_{OH}×0.7)/(n×0.01).

＜calculation example＞ I_{OH} = -10.0mA, n =80%

Total output current of pins = (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current at each pin does not vary due to duty cycle and does not flow above the absolute maximum rating.

Note: In N-channel open-drain mode, pins set to active N-channel open-drain do not output high.

Remark: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low level output Current [Note1]	I_{OL1}	P00~P06, P10~P17, P30, P31 P40~P47, P50~P57, P60~P67 P70~P77, P80~P87, P100~P102 P110~P111, P120, P130, P136 P137, P140~P147, P150~P157 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85℃	-	-	30 [Note2]	mA
			2.0V≤EV_{DD}≤5.5V 85~125℃	-	-	15 [Note2]	
		P00~P04, P40~P45, P120, P130 P136, P137, P140~P144, P150~P153 Total pins (at duty cycle≤70% [Note3])	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	100	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	50	
			2.4V≤EV_{DD}<4.0V	-	-	30	mA
			2.0V≤EV_{DD}<2.4V	-	-	15	mA
		P05, P06, P10~P17, P30, P31 P50~P55, P60~P67, P70~P77, P100 P110~P111, P146, P147 Total pins (at duty cycle≤70% [Note3]).	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	120	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	60	
			2.4V≤EV_{DD}<4.0V	-	-	40	mA
			2.0V≤EV_{DD}<2.4V	-	-	20	mA
		Total pins (at duty cycle≤70% [Note3])	2.0V≤EV_{DD}≤5.5V -40~85℃	-	-	150	mA
			2.0V≤EV_{DD}≤5.5V 85~125℃	-	-	80	
			2.4V≤EV_{DD}≤4.0V	-	-	50	
			2.0V≤EV_{DD}≤2.4V	-	-	30	
	I_{OL2}	P20 to P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	6 [Note2]	mA
		Total pins (at duty cycle≤70% [Note3])	2.0V≤V_{DD}≤5.5V	-	-	20	mA

Note 1: This is the current value at which the device is guaranteed to operate even if current flows from the output pin to the EV_{SS} and V_{SS} pins.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the "duty cycle ≤70% condition". The output current value of 70% is changed to a duty cycle ＞ can be calculated using the following calculation (if the duty cycle is changed to n%).

Total output current of pins = (I_{OL}×0.7)/(n×0.01).

＜calculation example ＞ I_{OL}= 10.0mA, n = 80%

Total output current of the pins = (10.0×0.7)/ (80×0.01) ≈ 8.7mA

The current at each pin does not vary due to duty cycle and does not flow above the absolute maximum rating.

Remark: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Power supply input voltage	V_{DD} EV_{DD}	-		2.0	-	5.5	V
The supply ground input voltage	V_{SS} EV_{SS}	-		-0.3	-	-	V
High input voltage	V_{IH1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P64~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P136 P140~7P147, P150~P157	Schmidt input	0.8EV_{DD}	-	EV_{DD}	V
	V_{IH2}	P01, P03, P04, P10 P14~P17, P30, P43~P44 P50, P55, P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	2.2	-	EV_{DD}	V
			TTL input 3.3V≤EV_{DD}<4.0V	2.0	-	EV_{DD}	V
			TTL input 2.0V≤EV_{DD}<3.3V	1.5	-	EV_{DD}	V
	V_{IH3}	P20~P27, P137		0.7V_{DD}	-	V_{DD}	V
	V_{IH4}	P60~P63		0.7EV_{DD}	-	6.0	V
	V_{IH5}	P121~P124, EXCLK, EXCLKS, RESETB		0.8V_{DD}	-	V_{DD}	V
Low input voltage	V_{IL1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P64~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P136 P140~P147, P150~P157	Schmidt input	0	-	0.2EV_{DD}	V
	V_{IL2}	P01, P03, P04, P10 P14~P17, P30, P43~P44 P50, P55, P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	0	-	0.8	V
			TTL input 3.3V≤EV_{DD}<4.0V	0	-	0.5	V
			TTL input 2.0V≤EV_{DD}<3.3V	0	-	0.32	V
	V_{IL3}	P20~P27, P137		0	-	0.3V_{DD}	V
	V_{IL4}	P60~P63		0	-	0.3EV_{DD}	V
	V_{IL5}	P121~P124, EXCLK, EXCLKS, RESETB		0	-	0.2V_{DD}	V

Note: Even in N-channel open-drain mode, the V_{IH} maximum value of the pin set to active N-channel open-drain is EV_{DD}.

Remarks: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level Output voltage	V_{OH1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P64~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P130 P136, P137, P140~P147 P150~P157	4.0V≤EV_{DD}≤5.5V, I_{OH1}= -12.0mA	EV_{DD}-1.5	-	-	V
			4.0V≤EV_{DD}≤5.5V, I_{OH1}= -6.0mA	EV_{DD}-0.7	-	-	V
			2.4V≤EV_{DD}≤5.5V, I_{OH1}= -3.0mA	EV_{DD}-0.6	-	-	V
			2.0V≤EV_{DD}≤5.5V, I_{OH1}= -2mA	EV_{DD}-0.5	-	-	V
	V_{OH2}	P20~P27	4.0V≤V_{DD}≤5.5V, I_{OH2}= -2.5mA	EV_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V, I_{OH2}= -1.5mA	EV_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V, I_{OH2}= -0.5mA	EV_{DD}-0.6	-	-	V
			2.0V≤V_{DD}≤5.5V, I_{OH2}= -0.4mA	V_{DD}-0.5	-	-	V
Low level Output voltage	V_{OL1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P60~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P130 P136, P137, P140~P147 P150~P157	4.0V≤EV_{DD}≤5.5V, I_{OL1}=30.0mA	-	-	1. 2	V
			4.0V≤EV_{DD}≤5.5V, I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤EV_{DD}≤5.5V, I_{OL1}=6.0mA	-	-	0.4	V
			2.0V≤EV_{DD}≤5.5V, I_{OL1}=4.0mA	-	-	0.4	V
	V_{OL2}	P20~P27	4.0V≤V_{DD}≤5.5V, I_{OL2}=6.0mA	-	-	1. 2	V
			4.0V≤V_{DD}≤5.5V, I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V, I_{OL2}=1.5mA	-	-	0.4	V
			2.0V≤V_{DD}≤5.5V, I_{OL2}=1.0mA	-	-	0.4	V

Note: In N-channel open-drain mode, pins set to active N-channel open-drain do not output high.

Remarks: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High input leakage current	I_{LIH1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P60~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P130 P136, P140~P147 P150~P157	V_I=EV_{DD}	-	-	1	uA
	I_{LIH2}	P20~P27, P137, RESETB	V_I=V_{DD}	-	-	1	uA
	I_{LIH3}	P121~P124 (X1, X2, EXCLK XT1, XT2, EXCLKS)	V_I=V_{DD}, when the input port and external clock are in	-	-	1	uA
			V_I=V_{DD}, when a resonator is connected	-	-	10	uA
Low input leakage current	I_{LIL1}	P00~P06, P10~P17, P30 P31, P40~P47, P50~P57 P60~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P130 P136, P140~P147 P150~P157	V_I=EV_{SS}	-	-	-1	uA
	I_{LIL2}	P20~P27, P137, RESETB	V_I=V_{SS}	-	-	-1	uA
	I_{LIL3}	P121~P124 (X1, X2, EXCLK XT1, XT2, EXCLKS)	V_I=V_{SS}, when entering the port and external clock input	-	-	-1	uA
			V_I=V_{SS}, when a resonator is connected	-	-	-10	uA
Internal pull-up resistor	R_U	P00~P06, P10~P17, P30 P31, P40~P45, P50~P57 P64~P67, P70~P77 P80~P87, P100~P102 P110~P111, P120, P136 P137, P140~P147	V_I=EV_{SS}, when entering the port	10	30	100	KΩ

Note: Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.

6.5.2 Supply Current Characteristics

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Mode	Clock	Condition		Min	Typ	Max	Unit
Supply current Note1	I_{DD1}	Run mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note3		-	7.5	18	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	7.5	16	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	9	14	
			High-speed master system clock	F_{MX}=20MHz Note2	Enter the square wave	-	6	12	mA
					Connect the crystal oscillator	-	6	12	
			The secondary system clock runs	F_{SUB}=32.768KHz Note4	Enter the square wave	-	80	200	uA
					Connect the crystal oscillator	-	80	200	
	I_{DD2}	sleep mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note3		-	2.4	12	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	1.8	10	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	1.2	8	
			High-speed master system clock	F_{MX}=20MHz Note2	Enter the square wave	-	1	4	mA
					Connect the crystal oscillator	-	1	4	
			The secondary system clock runs	F_{SUB}=32.768KHz Note5	Enter the square wave	-	1.8	100	uA
					Connect the crystal oscillator	-	1.8	100	
	I_{DD3} Note6	Deep sleep mode Note7		T_A= -40°C~25°C V_{DD}=3.0V		-	1.5	2.4	uA
				T_A= -40°C~85°C V_{DD}=3.0V		-	1.5	25	
				T_A= -40°C~105°C V_{DD}=3.0V		-	1.5	35	
				T_A= -40°C~125°C V_{DD}=3.0V		-	1.5	80	

Note1: This is the total current flowing through V_{DD} and EV_{DD}, including the input pins fixed as V_{DD}, EV_{DD} or the input leakage current of the V_{SS}, EV_{SS} status. Typical: The CPU is in the multiplication instruction execution (I_{DD1}) and does not contain peripheral operating currents. Maximum: The CPU is in the multiplication instruction execution (I_{DD1}) and contains peripheral operating current, but does not include the flow to the A/D converter the current in the LVD circuit, I/O ports, and internal pull-up or pull-down resistors does not include the current at which the data flash is

rewritten.

Note2: This is a case where the high-speed internal oscillator and subsystem clock stop oscillating.

Note3: This is a case where the high-speed master system clock and the sub-system clock stop oscillating.

Note4: This is a case where the high-speed internal oscillator and the high-speed master system clock stop oscillating.

Note5: This is a case where the high-speed internal oscillator and the high-speed master system clock stop oscillating. Contains current flowing to the RTC, but does not include current flowing to the 15-bit interval timer and watchdog timer.

Note6: Does not include current flowing to the RTC, 15-bit interval timer, and watchdog timer.

Note7: For the value of the current when the secondary system clock is running in deep sleep mode, refer to the current value when the secondary system clock is running in sleep mode.

Remark:

1. $F_{HOCO: The}$ clock frequency of the high-speed internal oscillator, F_{IH}: The system clock frequency provided by the high-speed internal oscillator.
2. $F_{SUB:}$ External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. F_{MX}: External master system clock frequency (X1/X2 clock oscillation frequency).
4. The Typical temperature condition is T_A = 25°C.

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low-speed internal oscillator operating current	I_{FIL} [Note1]	-	-	0.2	-	uA
RTC operating current	I_{RTC} [Note1,2,3]	-	-	0.04	-	uA
15-bit interval timer operating current	I_{IT} [Note1,2,4]	-	-	0.02	-	uA
Watchdog timer operating current	I_{WDT} [Note1,2,5]	F_{IL}=15KHz	-	0.22	-	uA
The A/D converter operates current	I_{ADC} [Note1,6]	ADC HS mode @64MHz	-	2.2	-	mA
		ADC HS mode @4MHz	-	1.3	-	mA
		ADC LC mode @24MHz	-	1.1	-	mA
		ADC LC mode @4MHz	-	0.8	-	mA
The D/A converter operates current	I_{DAC} [Note1.8]	Per channel	-	1.4	-	mA
PGA operating current		Per channel	-	480	700	uA
Comparator operating current	I_{CMP} [Note1, 9]	Per channel: The internal reference voltage is not used	-	60	100	uA
		Per channel: An internal reference voltage is used	-	80	140	uA
LVD operating current	I_{LVD} [Note1,7]	-	-	0.08	-	uA

Note1: This is the current flowing through V_{DD}.

Note2: This is a case where the high-speed internal oscillator and the high-speed system clock stop oscillating.

Note3: This is the current that only flows to the real-time clock (RTC) (excluding the operating current of the low-speed internal oscillator and XT1 oscillation circuitry). In the case of a real-time clock in operating or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{RTC}. In addition, when selecting a low-speed internal oscillator, I_{FIL} must be added. I_{DD2} when the secondary system clock is running contains the operating current of the real-time clock.

Note4: This is the current that only flows to the 15-bit interval timer (excluding the operating current of the low-speed internal oscillator and the XT1 oscillation circuit). With a 15-bit interval timer running in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus I_{IT}. In addition, when selecting a low-speed internal oscillator, I_{FIL} must be added.

Note5: This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). With the watchdog timer running, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{WDT}.

Note6: This is the current that only flows to the A/D converter. In either operating mode or sleep mode with the A/D converter running, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of the I_{ADC}.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus I the value of LVD.

Note8: This is the current that only flows to the D/A converter. In the case of the D/A converter in operating or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of the I_{DAC}.

Note9: This is the current that only flows to the comparator circuit. With the comparator circuit running, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{CMP}.

Remark:

1. F_{IL}: The clock frequency of the low-speed internal oscillator
2. The typical temperature condition is T_A = 25°C.

6.6 AC Characteristics

(T_A= -40~125˚C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Instruction period (minimum instruction execution time)	T_{CY}	The main system clock (F_{MAIN}) runs	2.0V≤V_{DD}≤5.5V	0.015625	-	1	us
		The secondary system clock (F_{SUB}) runs	2.0V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	2.0V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.0V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
The high- or low-level width of the external system clock input	T_{EXH}, T_{EXL}	2.0V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS}, T_{EXLS}	2.0V≤V_{DD}≤5.5V		13.7	-	-	us
TI00 ~ TI03, TI10 ~ TI17 input high- and low-level width	T_{TIH}, T_{TO}	2.0V≤V_{DD}≤5.5V		1/F_{MCK}+10	-	-	ns
The input period of the timer TimerA	T_C	T_{AIO}	2.4V≤EV_{DD}≤5.5V	100	-	-	ns
			2.0V≤EV_{DD}<2.4V	300	-	-	ns
The high- and low-level width of the timer TimerA input	T_{TAIH}, T_{TAIL}	T_{AIO}	2.4V≤EV_{DD}≤5.5V	40	-	-	ns
			2.0V≤EV_{DD}<2.4V	120	-	-	ns

Remark: F_{MCK}: Timer4, Timer8 unit operating clock frequency.

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
The high or low level width of the M input of the timer	T_{TMIH}, T_{TMIL}	TMIOA0, TMIOA1, TMIOB0, TMIOB1 TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/F_{CLK}	-	-	ns
Timer M forces the cutoff of the low width of the signal input	T_{TMSIL}	P136/INTP0	2MHz<F_{CLK}≤48MHz	1	-	-	us
			F_{CLK}≤2MHz	1/F_{CLK}+1	-	-	us
The high and low level width of the timer B input	T_{TBIH}, T_{TBIL}	TBIOA, TBIOB		2.5/F_{CLK}	-	-	ns
Output frequencies of TO00 ~ TO03, TO10 ~ TO17, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB	F_{TO}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}<4.0V		-	-	8	MHz
		2.0V≤EV_{DD}<2.4V		-	-	4	MHz
Output frequencies of CLKBUZ0 and CLKBUZ1	F_{PCL}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}<4.0V		-	-	8	MHz
		2.0V≤EV_{DD}<2.4V		-	-	4	MHz
The high- and low-level width of the interrupt input	T_{INTH}, T_{INTL}	INTP0~INTP11	2.0V≤EV_{DD}≤5.5V	1	-	-	us
The key interrupts the high or low level width of the input	T_{KR}	KR0 ~KR7	2.0V≤EV_{DD}≤5.5V	250	-	-	ns
The low-level width of RESETB	T_{RSL}	-		10	-	-	us

6.7 Peripheral Features

6.7.1 Universal Interface Unit

(1) UART mode

(T_A= -40~85°C、2.0V≤EV_{DD}=V_{DD}≤5.5V、V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value		Unit
			Min	Max	
Transfer rate	2.0V≤EV_{DD}≤5.5V	-	-	F_{MCK}/6	bps
		The theoretical value of the maximum transfer rate, F_{MCK}=F_{CLK}	-	10.6	Mbps

(T_A=85~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value		Unit
			Min	Max	
Transfer rate	2.0V≤EV_{DD}≤5.5V	-	-	F_{MCK}/12	bps
		The theoretical value of the maximum transfer rate, F_{MCK}=F_{CLK}	-	5.3	Mbps

(2) Three-wire SPI mode (master mode, internal clock output).

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85°C		85~125°C		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ≥ 2/F_{CLK}	4.0V≤EV_{DD}≤5.5V	31.25	-	62.5	-	ns
			2.7V≤EV_{DD}≤5.5V	41.67	-	83.33	-	ns
			2.4V≤EV_{DD}≤5.5V	65	-	125	-	ns
			2.0V≤EV_{DD}≤5.5V	125	-	250	-	ns
SCLKp high/low level width	T_{KH1} T_{KL1}	4.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-4	-	T_{KCY1}/2-7	-	ns
		2.7V≤EV_{DD}≤5.5V		T_{KCY1}/2-5	-	T_{KCY1}/2-10	-	ns
		2.4V≤EV_{DD}≤5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
		2.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-19	-	T_{KCY1}/2-38	-	ns
SDIp preparation time (to SCLKp↑).	T_{SIK1}	4.0V≤EV_{DD}≤5.5V		12	-	23	-	ns
		2.7V≤EV_{DD}≤5.5V		17	-	33	-	ns
		2.4V≤EV_{DD}≤5.5V		20	-	38	-	ns
		2.0V≤EV_{DD}≤5.5V		28	-	55	-	ns
SDIp hold time (to SCLKp↑).	T_{KSI1}	2.0V≤EV_{DD}≤5.5V		5	-	10	-	ns
SCLKp↓→ SDOp output delay time	T_{KSO1}	2.0V≤EV_{DD}≤5.5V C=20pF Note1		-	5	-	10	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Note: The SDIp pin is selected as the usual input buffer and the SDOp pin and SCLKp pin are selected as the usual output mode through the port input mode register and the port output mode register.

Remark: Guaranteed by design, mass production is not tested.

(3) Three-wire SPI mode (slave mode, external clock input).

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85°C		85~125°C		Unit
				Min	Max	Min	Max	
SCLKp Cycle time	T_{KCY2}	4.0V≤EV_{DD} ≤5.5V	20MHz<F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V≤EV_{DD} ≤5.5V	16MHz<F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V≤EV_{DD}≤5.5V		6/F_{MCK} and ≥500	-	12/F_{MCK} and ≥1000	-	ns
		2.0V≤EV_{DD}≤5.5V		6/F_{MCK} and ≥750	-	12/F_{MCK} and ≥1500	-	ns
SCLKp High/low level width	T_{KH2} T_{KL2}	4.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V≤EV_{DD}≤5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		2.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp Preparation time (to SCLKp↑).	T_{SIK2}	2.7V≤EV_{DD}≤5.5V		1/F_{MCK}+20	-	1/F_{MCK}+40	-	ns
		2.0V≤EV_{DD}≤5.5V		1/F_{MCK}+30	-	1/F_{MCK}+60	-	ns
SDIp Hold time (to SCLKp↑).	T_{KSI2}	2.0V≤EV_{DD}≤5.5V		1/F_{MCK}+31	-	1/F_{MCK}+62	-	ns
SCLKp↓ → the SDOp output delay time	T_{KSO2}	2.7V≤EV_{DD}≤5.5V, C=30pF Note1		-	2/F_{MCK}+ 44	-	2/F_{MCK}+ 66	ns
		2.4V≤EV_{DD}≤5.5V, C=30pF Note1		-	2/F_{MCK}+ 75	-	2/F_{MCK}+ 113	ns
		2.0V≤EV_{DD}≤5.5V, C=30pF Note1		-	2/F_{MCK}+ 100	-	2/F_{MCK}+ 150	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Note: The SDIp pin and SCLKp pin are selected as the usual input buffers and the SDOp pin is selected as the usual output mode through the port input mode register and the port output mode register.

Remark: Guaranteed by design, mass production is not tested.

(4) Four-wire SPI mode (slave mode, external clock input).

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85°C		85~125°C		Unit
				Min	Max	Min	Max	
SSI00 Establishment time	T_{SSIK}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	$1/F_{MCK}$+120	-	$1/F_{MCK}$+240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	$1/F_{MCK}$+200	-	$1/F_{MCK}$+400	-	ns
SSI00 Hold time	T_{KSSI}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	$1/F_{MCK}$+120	-	$1/F_{MCK}$+240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	$1/F_{MCK}$+200	-	$1/F_{MCK}$+400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns

Note: The SDIp pin and SCLKp pin are selected as the usual input buffers and the SDOp pin is selected as the usual output mode through the port input mode register and the port output mode register.

Remark: Guaranteed by design, mass production is not tested.

(5) Simple IIC mode

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	-40~85°C		85~125°C		Unit
			Min	Max	Min	Max	
SCLr clock frequency	F_{SCL}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	-	1000 Note1	-	400 Note1	KHz
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	-	400 Note1	-	100 Note1	KHz
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	-	300 Note1	-	75 Note1	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475	-	1200	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150	-	4600	-	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Data settling time (received)	$T_{SU: THAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	1/F_{MCK}+85 Note2	-	1/F_{MCK}+ 220 Note2	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1/F_{MCK}+145 Note2	-	1/F_{MCK}+ 580 Note2	-	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1/F_{MCK}+230 Note2	-	1/F_{MCK}+ 1200 Note2	-	ns
Data Hold Time (Send)	$T_{HD: DAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	305	-	770	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	-	355	-	1420	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	405	-	2070	ns

Note 1: Must be set to at least F_{MCK}/4.

Note 2: The setpoint of the F_{MCK} cannot exceed the hold times of SCLr="L" and SCLr="H".

Remark: Guaranteed by design, mass production is not tested.

6.7.2 Serial Interface IICA

(1) I²C standard mode

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
The time at which the startup condition was established	$T_{SU:STA}$	-	4.7	-	us
Hold time of the startup condition Note1	$T_{HD:STA}$	-	4.0	-	us
When SCLAr is low, hold time	T_{LOW}	-	4.7	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	4.0	-	us
Data settling time (received)	$T_{SU:THAT}$	-	250	-	ns
Data Hold Time (Send) Note2	$T_{HD:DAT}$	-	0	3.45	us
The time at which the stop condition was established	$T_{SU:STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note 1: The first clock pulse is generated after the start condition or restart condition is generated.

Note 2: The maximum value of $T_{HD:DAT}$ needs to be guaranteed during normal transmission, and it is necessary to wait for the answer (ACK) to be performed.

Note: The maximum value of C_b (communication line capacitance) for each mode and R_b (the pull-up resistance value of the communication line) at this time are as follows:

standard mode：C_b=400pF, R_b=2.7KΩ

(2) I²C fast mode

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
The time at which the startup condition was established	$T_{SU:\ STA}$	-	0.6	-	us
Hold time of the startup condition Note1	$T_{HD:\ STA}$	-	0.6	-	us
When SCLAr is low, hold time	T_{LOW}	-	1.3	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	0.6	-	us
Data settling time (received)	$T_{SU:\ THAT}$	-	100	-	ns
Data Hold Time (Send) Note2	$T_{HD:\ DAT}$	-	0	0.9	us
The time at which the stop condition was established	$T_{SU:\ STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note 1: The first clock pulse is generated after the start condition or restart condition is generated.

Note 2: The maximum value of $T_{HD:DAT}$ needs to be guaranteed during normal transmission, and it is necessary to wait for the answer (ACK) to be performed.

Note: The maximum value of C_b (communication line capacitance) for each mode and R_b (the pull-up resistance value of the communication line) at this time are as follows:

Fast mode：C_b=320pF, R_b=1.1KΩ

(3) I^2C Enhanced fast Mode

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Enhanced Fast Mode: F_{CLK}≥10MHz	-	1000	KHz
The time at which the startup condition was established	$T_{SU: STA}$	-	0.26	-	us
Hold time of the startup condition Note1	$T_{HD: STA}$	-	0.26	-	us
When SCLAr is low, hold time	T_{LOW}	-	0.5	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	0.26	-	us
Data settling time (received)	$T_{SU: THAT}$	-	50	-	ns
Data Hold Time (Send) Note2	$T_{HD:DAT}$	-	0	0.45	us
The time at which the stop condition was established	$T_{SU: STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note 1: The first clock pulse is generated after the start condition or restart condition is generated.

Note 2: The maximum value of $T_{HD:DAT}$ needs to be guaranteed during normal transmission, and it is necessary to wait when performing a reply (ACK).

Note: The maximum value of C_b (communication line capacitance) for each mode and R_b (the pull-up resistance value of the communication line) at this time are as follows:

Enhanced Fast Mode: C_b=120pF, R_b=1.1KΩ

6.8 Analog Characteristics

6.8.1 A/D Converter Features

Differentiation of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage (+) =AV_{REFF} Reference voltage (-) =AV_{REFM}	Reference voltage (+) =V_{DD} Reference voltage (-) =V_{SS}
ANI0~ ANI20	Refer to 6.8.1 (1)	Refer to 6. 8.1 (2)
The internal reference voltage, the output voltage of the temperature sensor		

(1) Select the case for reference voltage(+)=AV_{REFP}/ANI0 and reference voltage(-)=AV_{REFM}/ANI1 (T_A= -40~125°C, 2.0V≤AV_{REFP}≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=0V, reference voltage(+)=AV_{REFP}, Reference voltage(-)=AV_{REFM}=0V).

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion objects: ANI2~ ANI15	2.0V ≤V_{DD}≤ 5.5V	45	-	-	$1/F_{ADC}$
		12-bit resolution Conversion objects: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V ≤V_{DD}≤ 5.5V	72	-	-	$1/F_{ADC}$
External input resistance	R_{AIN}	R_{AIN} < $(Ts / (F_{ADC} \times C_{ADC} \times \ln(2^{12+2})) - R_{ADC})$		-	7.5 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitor	C_{ADC}	-		-	2		pF
		ANI2~ ANI15		0	-	AV_{REFP}	V

Analog input voltage	V_{AIN}	Internal reference voltage (2.0V≤V_{DD}≤5.5V).	V_{BGR} Note2	V
		The output voltage of the temperature sensor (2.0 V≤V_{DD}≤5.5V).	V_{TMPS25} Note2	V

Note 1: Quantization error is not included (± 1/2 LSB).

Note 2: Please refer to "6.8.2 Characteristics of Temperature Sensors/Internal Reference Voltages".

Note 3: The F_{ADC} is the operating frequency of the AD, with a maximum operating frequency of 64MHz.

Note 4: Mass production is not tested as guaranteed by design. The typical value is the default sampling period Ts=13.5, and the conversion speed is F_{ADC}=64MHz.

(2) Select the case where reference voltage (+) =V_{DD} and reference voltage (-) = V_{SS} are selected (T_A = -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤ 5.5V, V_{SS} =EV_{SS}=0V, Reference Voltage (+)=V_{DD}, Reference voltage (-) = V_{SS}).

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	-	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	-	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	-	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-2	-	2	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-3	-	3	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion objects: ANI0 ~ ANI15	2.0V≤V_{DD}≤5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion objects: internal reference voltage, output voltage of temperature sensor,	2.0V≤V_{DD}≤5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} < (T_s / (F_{ADC} x C_{ADC} x ln(2^{12+2})) - R_{ADC})		-	7.5 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitor	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ ANI7		0	-	V_{DD}	V
		ANI8~ ANI15		0	-	EV_{DD}	V
		Internal reference voltage (2.0V≤V_{DD}≤5.5V).		V_{BGR} Note2			V
		The output voltage of the temperature sensor (2.0V≤V_{DD}≤5.5V).		V_{TMPS25} Note2			V

Note 1: Quantization error is not included (± 1/2 LSB).

Note 2: Please refer to "6.8.2 Characteristics of Temperature Sensors/Internal Reference Voltages".

Note 3: The F_{ADC} is the operating frequency of the AD, with a maximum operating frequency of 64MHz.

Note 4: Mass production is not tested as guaranteed by design. The typical value is the default sampling period Ts=13.5, and the conversion speed is F_{ADC}=64MHz.

6.8.2 Characteristics of the Temperature Sensor/Internal Reference Voltage

(T_A = -40~125°C, 2.0V≤V_{DD}≤5.5V, V_{SS} =EV_{SS} =0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The output voltage of the temperature sensor	V_{TMPS25}	T_A =25°C	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A = -40~10°C	1.25	1.45	1.65	V
		T_A =10~70°C	1.38	1.45	1.52	V
		T_A =70~125°C	1.35	1.45	1.55	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/°C
Run stable wait time	T_{AMP}	-	5	-	-	us

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.8.3 D/A Converter

(T_A = -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS} =EV_{SS} =0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-	-	-	-	8	bit
Combined error	ET	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	-2.5	-	2.5	LSB
Stabilization time	T_{SET}	Cload=20pF	2.7V≤V_{DD}≤5.5V	-	-	3	us
			2.0V≤V_{DD}<2.7V	-	-	6	us
Output impedance	RO	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	4.7	-	8	KΩ

6.8.4 Comparator

(T_A = -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS} =EV_{SS} =0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	-	-	±10	±40	mV
Input voltage range	V_{IN}	-	0	-	V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register: 7FH to 80H (m = 0, 1).	-	-	±2	LSB
		other	-	-	±1	LSB
Response time	T_{CR}, T_{CF}	The input amplitude ± 100mV	-	70	125	ns
Run settling time Note1	T_{STB}	CMPn =0-＞1, V_{DD}= 3.3 ~5.5V	-	-	1	us
		CMPn =0-＞1, V_{DD}= 2.0 ~ 3.3V	-	-	3	us
Reference settling time	T_{VR}	CVRE=0-＞1 Note2	-	-	20	us
Operating current	I_{CMPDD}	Refer to 6.5.2 Supply current characteristics				

Note1: The time required from comparator action enable (CMPnEN=0 -＞1) to meeting the various DC/AC style requirements of CMP.

Note2: By setting the CVREm bit to 1; m = 0 to 1), the reference settling time is passed before the comparator output can be enabled (CnOE bit = 1; n = 0 to 1)

6.8.5 Programmable Gain Amplifier PGA

(T_A = -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS} =EV_{SS} =0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input deviation voltage	V_{IOPGA}	-		-	-	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xV_{DD}/Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xV_{DD}	-	-	V
	V_{IOLPGA}	-		-	-	0.07xV_{DD}	V
Gain deviation	-	x4	-	-	-	±1	%
		x8	-	-	-	±1	%
		x10	-	-	-	±1	%
		x12	-	-	-	±2	%
		x14	-	-	-	±2	%
		x16	-	-	-	±2	%
		x32	-	-	-	±3	%
Conversion rate Note2	SR_{RPGA}	Rise Vin= 0.1 V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% output voltage amplitude	4.0V ≤V_{DD}≤5.5 V (except x32)	3.5	-	-	V/us
			4.0 V ≤V_{DD}≤5.5 V (x32)	3.0	-	-	
			2.0 V ≤V_{DD}≤4.0V	0.5	-	-	
	SR_{FPGA}	Drop Vin= 0.1 V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% output voltage amplitude	4.0V ≤V_{DD}≤5.5 V (except x32)	3.5	-	-	
			4.0 V ≤V_{DD}≤5.5V (x32)	3.0	-	-	
			2.0 V ≤V_{DD}≤4.0V	0.5	-	-	
Stable operation to the time Note1	T_{PGA}	x4	-	-	-	5	us
		x8	-	-	-	5	us
		x10	-	-	-	5	us
		x12	-	-	-	10	us
		x14	-	-	-	10	us
		x16	-	-	-	10	us
		x32	-	-	-	10	us
Operating current	I_{PGADD}	Refer to 6.5.2 Supply current characteristics					

Note 1: The time required from PGA action enable (PGAEN=1) to meeting the various DC and AC style requirements of the PGA.

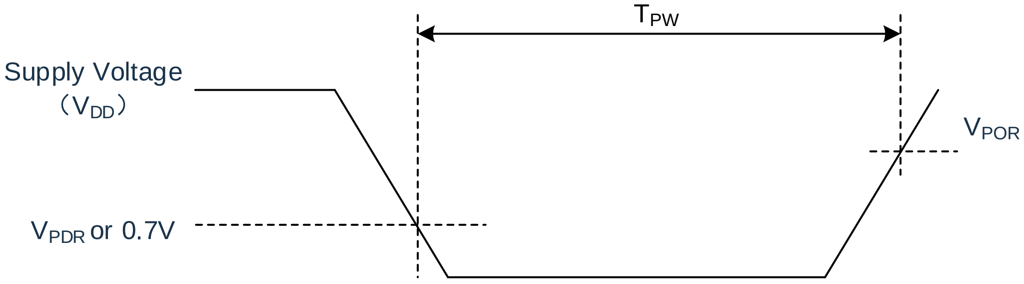
Note 2: Guaranteed by design, mass production is not tested.

6.8.6 POR Circuit Characteristics

(T_A = -40~125°C, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{BY}	When the supply voltage rises	-	1.50	2.0	V
	V_{PDR}	When the supply voltage drops	1.37	1.45	-	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	us

Note 1: This is the time required for the POR to reset when V_{DD} is lower than V_{PDR}. In addition, bit0 (HIOSTOP) and bit7() of the clock operating state control register (CSC) are set in deep sleep mode MSTOP) stops the oscillation of the main system clock (F_{MAIN}) from V_{DD} below 0.7V to a rebound above V The time required for POR reset up to POL.



6.8.7 LVD Circuit Characteristics

1. Reset mode, interrupt mode

(T_A= -40~125°C, $V_{PDR} \leqslant V_{DD} \leqslant 5.5V$, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD3}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD4}	When the supply voltage rises	-	2.09	2.16	V
		When the supply voltage drops	1.97	2.04	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

2. Interrupt mode or reset mode

(T_A= -40~125°C, $V_{PDR} \leqslant V_{DD} \leqslant 5.5V$, V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
Interrupt & Reset mode	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 0, 1, Drop the reset voltage			1.78	1.84	-	V
	V_{LVDB2}		LVIS1, LVIS0=0, 1	Rise reset release	-	2.09	2.16	V
				Drop the interrupt	1.97	2.04	-	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 0, Drop the reset voltage			-	2.45	-	V
	V_{LVDC2}		LVIS1, LVIS0=0, 1	Rise reset release	-	2.71	-	V
				Drop the interrupt	-	2.65	-	V
	V_{LVDC3}		LVIS1, LVIS0=0, 0	Rise reset release	-	3.75	-	V
				Drop the interrupt	-	3.67	-	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 1, Drop the reset voltage			-	2.75	-	V
	V_{LVDD2}		LVIS1, LVIS0=0, 1	Rise reset release	-	3.02	-	V
				Drop the interrupt	-	2.96	-	V
	V_{LVDD3}		LVIS1, LVIS0=0, 0	Rise reset release	-	4.06	4.26	V
				Drop the interrupt	3.78	3.98	-	V

6.8.8 Reset Time Versus Rising Slope Characteristics of The Supply Voltage

(T_A= -40~125°C, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Reset time	T_{RESET}	-	-	2	-	ms
The rising slope of the supply voltage	S_{VDD}	-	-	-	54	V/ms

6.9 Memory Characteristics

6.9.1 Flash Memory

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Test the conditions	Min	Max	Unit
T_{PROG}	Word Write Time (32bit)	T_A= -40~125°C	24	30	us
T_{ERASE}	Sector erase time	T_A= -40~125°C	4	5	ms
	Slice erase time	T_A= -40~125°C	20	40	ms
N_{END}	The number of times it can be erased	T_A= -40~125°C	100	-	Kcycle
T_{RET}	Data retention period	100 千次 Note1 at T_A = 125°C	20	-	years

Note 1: Cycle testing is performed over the entire temperature range.

Remark: Guaranteed by design, mass production is not tested.

6.9.2 RAM Storage

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Test the conditions	Min	Max	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A = -40~125°C	0.8	-	V

6.10 EMS Features

6.10.1 ESD Electrical Characteristics

Symbol	Parameter	Test the conditions	Class
$V_{ESD(HBM)}$	Electrostatic discharge (Human Discharge Mode HBM)	T_A=25°C JEDEC EIA/JESD22- A114	TBD

Remark: Guaranteed by design, mass production is not tested.

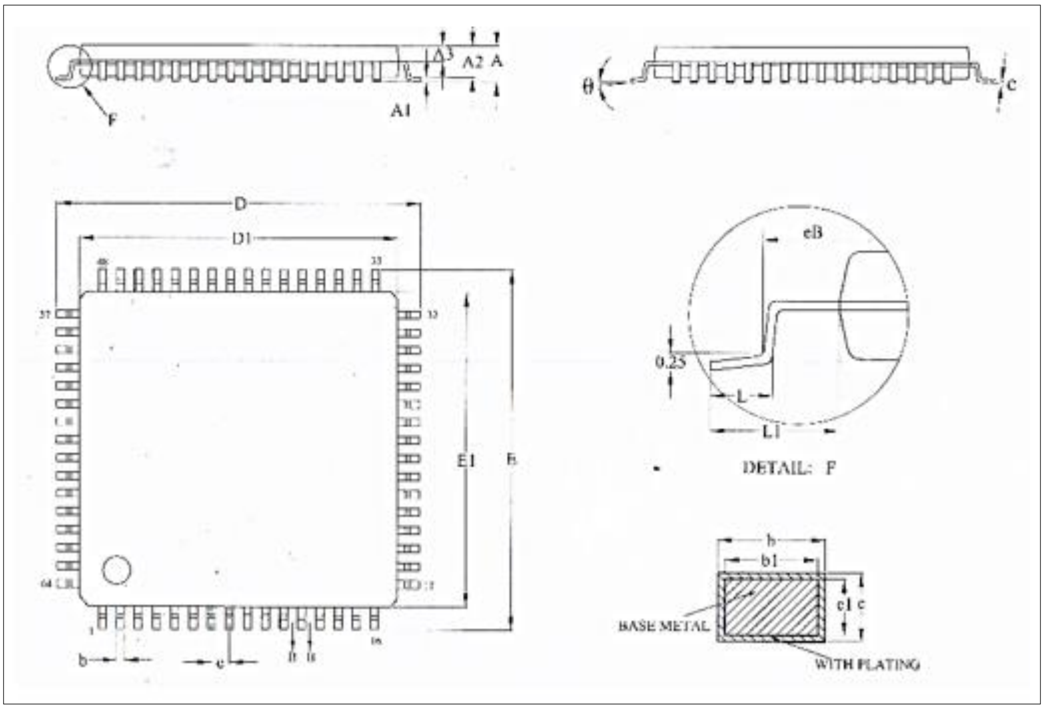
6.10.2 Latch-up Electrical Characteristics

Symbol	Parameter	Test the conditions	Class
LU	Static latch-up class	JEDEC STANDARD NO.78E NOVEMBER 2016	TBD

Remark: Guaranteed by design, mass production is not tested.

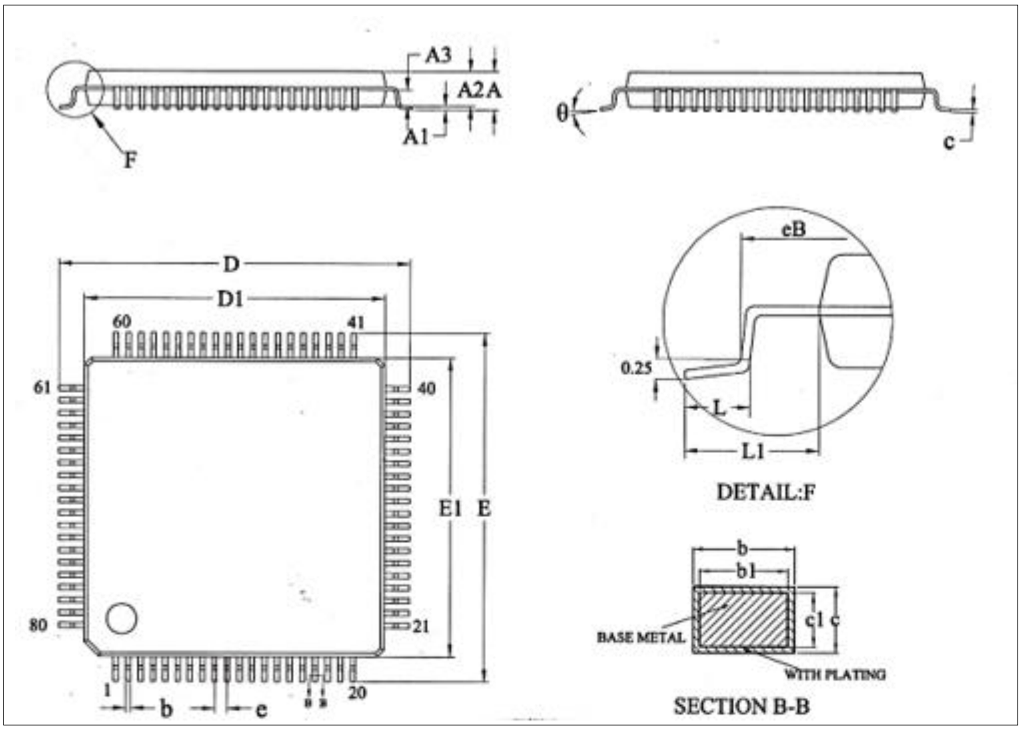
7 Package Information

7.1 LQFP64(7x7mm,0.4mm pitch).



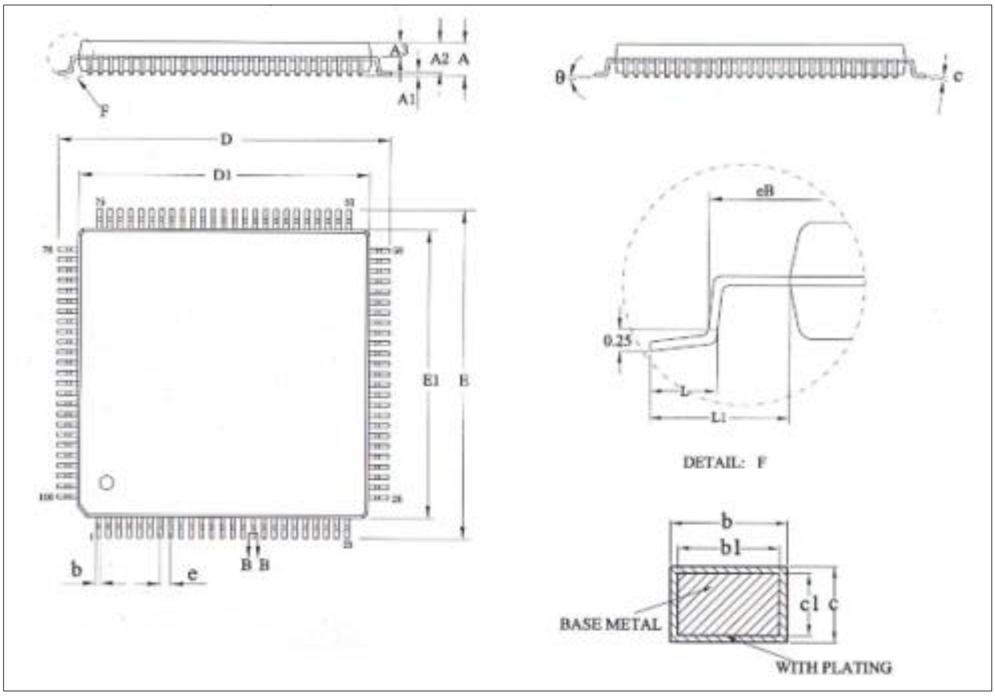
Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.2 LQFP80(12x12 mm,0.5mm pitch)



Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	-	7°

7.3 LQFP100(14x14mm,0.5mm pitch).



Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15. 35
e	0. 50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

8 Revision History

Version	Date	Modify content
V1.00	August 2022	Initial version
V1.01	Nov 2022	Modified the parameters in 6.5.1