BAT32G139 datasheet

ARM® Cortex®-M0+ based, ultra low power consumption 32-bit microcontroller

Built-in 256K byte Flash, rich simulation function, timer and various communication interfaces

V1.3

Features

- **Ultra-low power consumption operating environment:**
  - Power supply voltage range:1.8V to 5.5V
  - Temperature range: -40℃ to 105℃
  - Low power consumption mode: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz@64MHz
  - Power consumption in deep sleep mode: 0.8uA
  - Deep sleep mode +32.768K+RTC: 1.2uA
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Working frequency: 32KHz～64MHz
- **Memory:**
  - 256KB Flash memory, with program and data storage shared
  - 2.5KB dedicated data Flash memory
  - 32KB SRAM memory with parity check
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management:**
  - Built-in high-speed vibrator, accuracy (±1%). Can provide 1MHz～64MHz system clock and peripheral module operation clock
  - Built-in 15KHz low-speed oscillator
  - Built-in 1 PLL
  - Support 1MHz～20MHz external crystal oscillator
  - Support 32.768KHz external crystal oscillator, which can be used to calibrate internal high-speed oscillator
- **Multiplier/divider module:**
  - Multiplier: Support single cycle 32bit multiplication operation
  - Divider: Support 32bit signed integer division operation, only 8 CPU clock cycles to complete an operation
- **Enhanced DMA controller:**
  - Interrupt trigger start
  - Transmission mode is selectable (normal transmission mode, repeated transmission mode, block transmission mode and chain transmission mode)
  - The transmission source/destination area is optional for the full address space range
- **Linkage controller:**
  - The event signals can be linked together to realize the linkage of peripheral functions.
  - 15 types of event input, 10 types of event trigger.
- **Abundant analog peripheral:**
  - 12-bit precision ADC converter, conversion rate 1.42Msps, 21 external analog channels, internal optional PGA output as conversion channel, with temperature sensor, support single-channel conversion mode and multi-channel scan conversion mode Conversion range: 0 to positive reference voltage
  - 8-bit precision D/A converter, 2-channel analog output, real-time output function, output voltage range 0~VDD
  - Comparator (CMP), built-in two-channel comparator with hysteresis, optional input source, reference voltage can be external reference voltage or internal reference voltage
  - Programmable gain amplifier (PGA), built-in two-channel PGA, can set 4/8/10/12/14/16/32 times gain, with external GND pin (can be used as differential mode)
- **Input/output port:**
  - Number of I/O port: 41～71
  - Can switch between N-channel open drain, TTL input buffer and internal pull-up and pull-down
  - Built-in button interrupt detection function
  - Built-in clock output/buzzer output control circuit
- **Serial two-wire debugger (SWD)**
- **Abundant timer:**
  - 16-bit timer: 17 channels (With PWM function and motor dedicated PWM function)
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer (WWDT): 1
  - SysTick timer
- **Abundant and flexible interface:**
  - 4-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simple I2C
  - Standard I2C：2 channels
  - CAN:2 channel

- **security function:**
  - Comply with relevant standards of IEC/UL 60730
  - Abnormal storage space access error
  - Support RAM parity check
  - Support hardware CRC check
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Flash secondary protection in debug mode (level1: only the entire flash area can be erased, not read or write; level2: the emulator connection is invalid, and the flash operation is not possible)
- **Encapsulation:**
  - Support multiple encapsulations of 48Pin, 64Pin and 80Pin

1 Overview

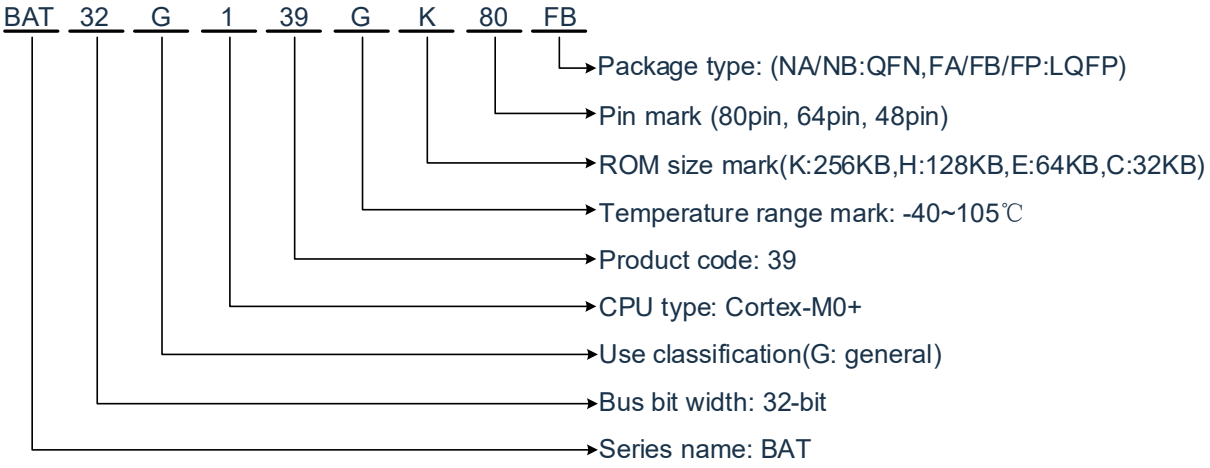
1.1 Introduction

Ultra-low power consumption BAT32G139 uses high-performance 32-bit RISC core of ARM®Cortex®-M0+, can work at a frequency of up to 64 MHz, and adopts high-speed embedded flash memory (SRAM max. 32KB, program/data flash memory max. 256KB). This product integrates multiple standard interfaces of I2C, SPI, UART, LIN and CAN bus Integrated 12bit A/D converter, temperature sensor, 8bitD/A converter, comparator, programmable gain amplifier. Among them, the 12bit A/D converter can collect external sensor signals, reducing system design costs. 8bit D/A converter can be used for audio playback or power control. The temperature sensor integrated in the chip can realize real-time monitoring of the external ambient temperature. The internally integrated comparator of the chip can support both high-speed and low-speed operating modes. In the high-speed mode, it can support the control feedback of the high-speed motor, and in the low-speed mode, it can be used for battery monitoring. Integrate a variety of advanced timer modules, load 1-channel SysTick timer, 17-channel 16bit timer, 1-channel 15bit interval timer, watchdog timer and real-time clock and other functions, and can support general-purpose PWM and motor-specific PWM applications.

BAT32G139 also has excellent low-power performance, supports two low-power modes of sleep and deep sleep, and is designed to be flexible. Its operating power consumption is 120uA/MHz@64MHz, and the power consumption is only 0.8uA in deep sleep mode, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without the intervention of the CPU, which is faster than using interrupt response, while reducing the frequency of CPU activity and prolonging the battery life.

These characteristics make the BAT32G139 microcontroller series can be widely used in various application scenarios, such as automotive body control, motor drive control, household appliances and mobile devices and other high-performance low-power applications.

1.2 Product model list



List of products of BAT32G139:

Number of Pin	Encapsulation	Product model
48-pin	48-pin plastic package LQFP (7×7mm，0.5mm pitch)	BAT32G139GK48FA
64-pin	64-pin plastic package LQFP (7×7mm，0.4mm pitch)	BAT32G139GK64FB
80-pin	80-pin plastic package LQFP (12×12mm，0.5mm pitch)	BAT32G139GK80FA

FLASH, SRAM capacity:

Flash memory	Special data Flash memory	SRAM	BAT32G139		
			48-pin	64-pin	80-pin
256KB	2.5KB	32KB	BAT32G139GK48	BAT32G139GK64	BAT32G139GK80

1.3 Pin connection diagram (Top View)

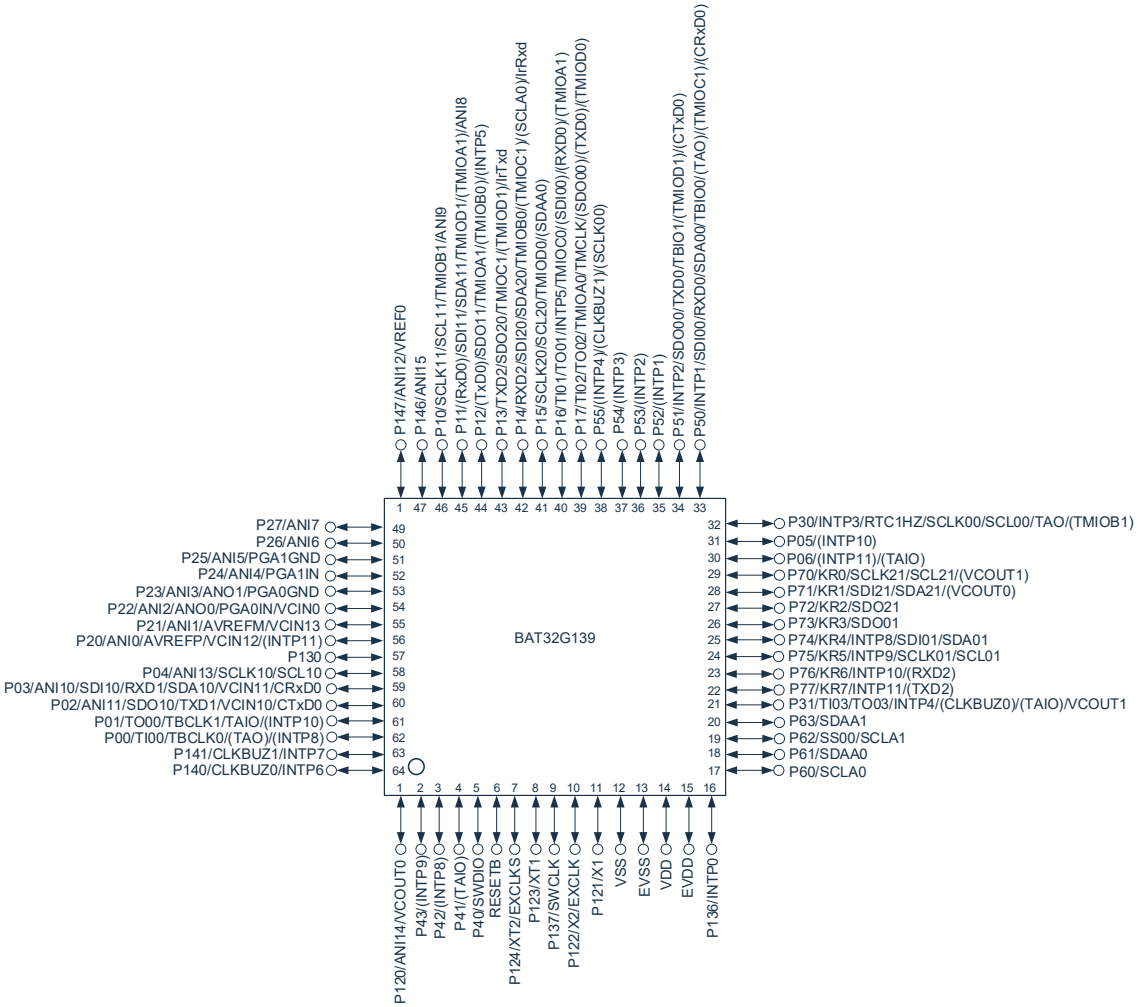
1.3.1 48-pin product

- 48-pin plastic package LQFP(7x7mm, 0.5mm pitch)

Note: The functions in the above figure () can be allocated by setting the peripheral I/O redirection register.

1.3.2 64-pin product

- 64-pin plastic package LQFP(7x7mm, 0.4mm pitch)

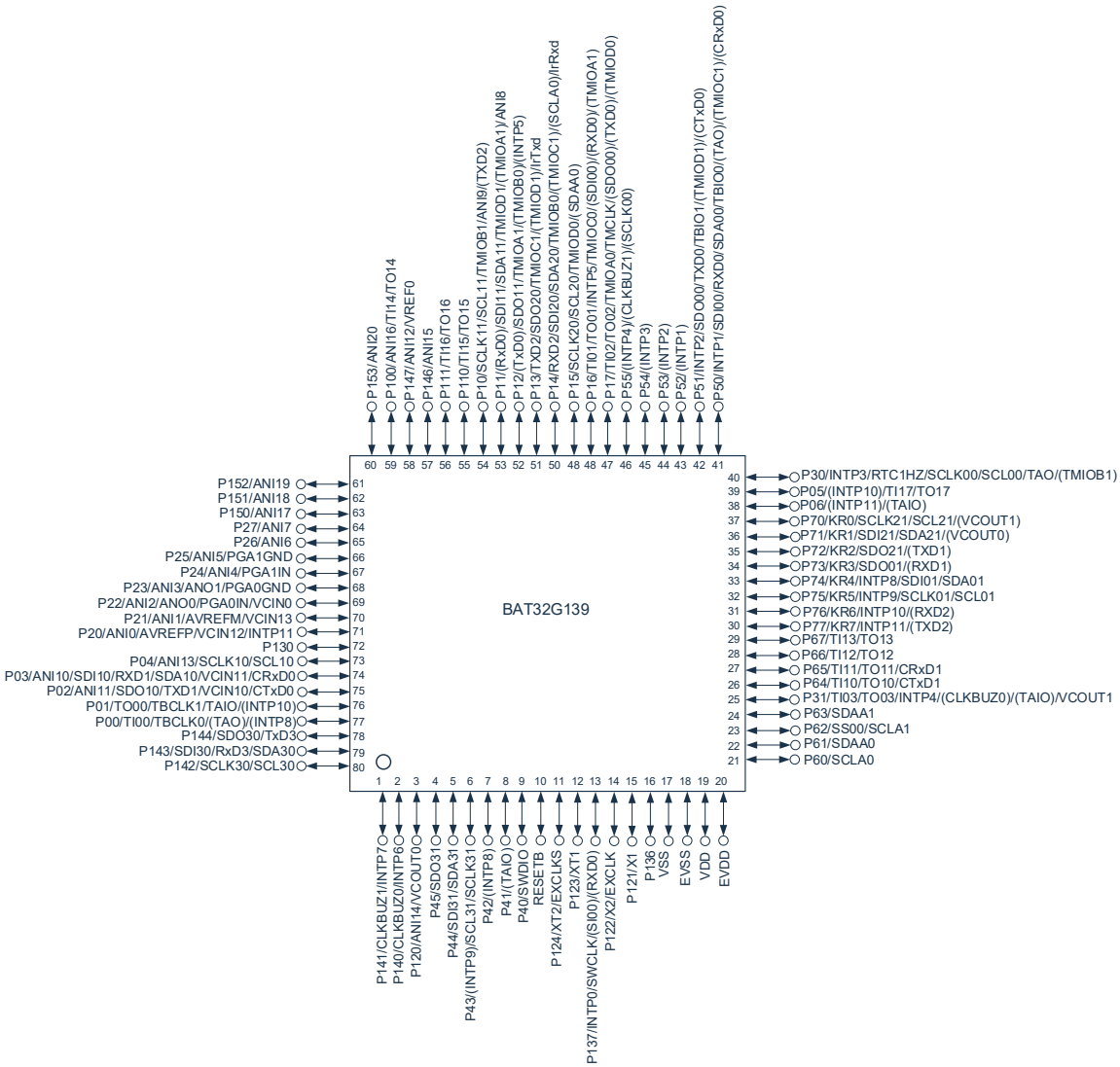


Note:

1) Make EVSS pin the same potential as VSS pin.
2) Make EVDD pin the same potential as VDD pin.
3) When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separateground lines.
4) Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.3 80-pin product

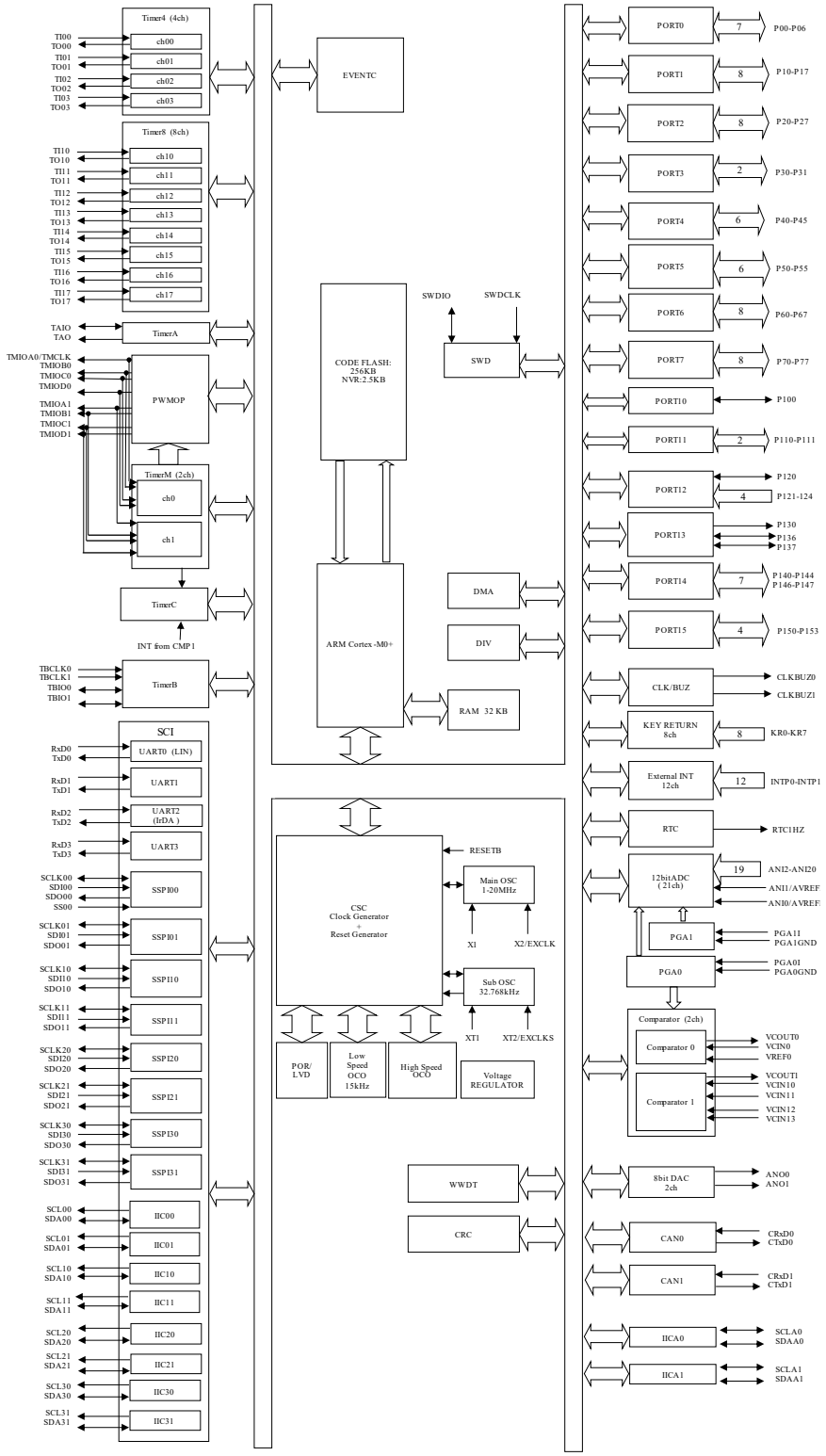
- 80-pin plastic package LQFP(12x12mm, 0.5mm pitch)



Note:

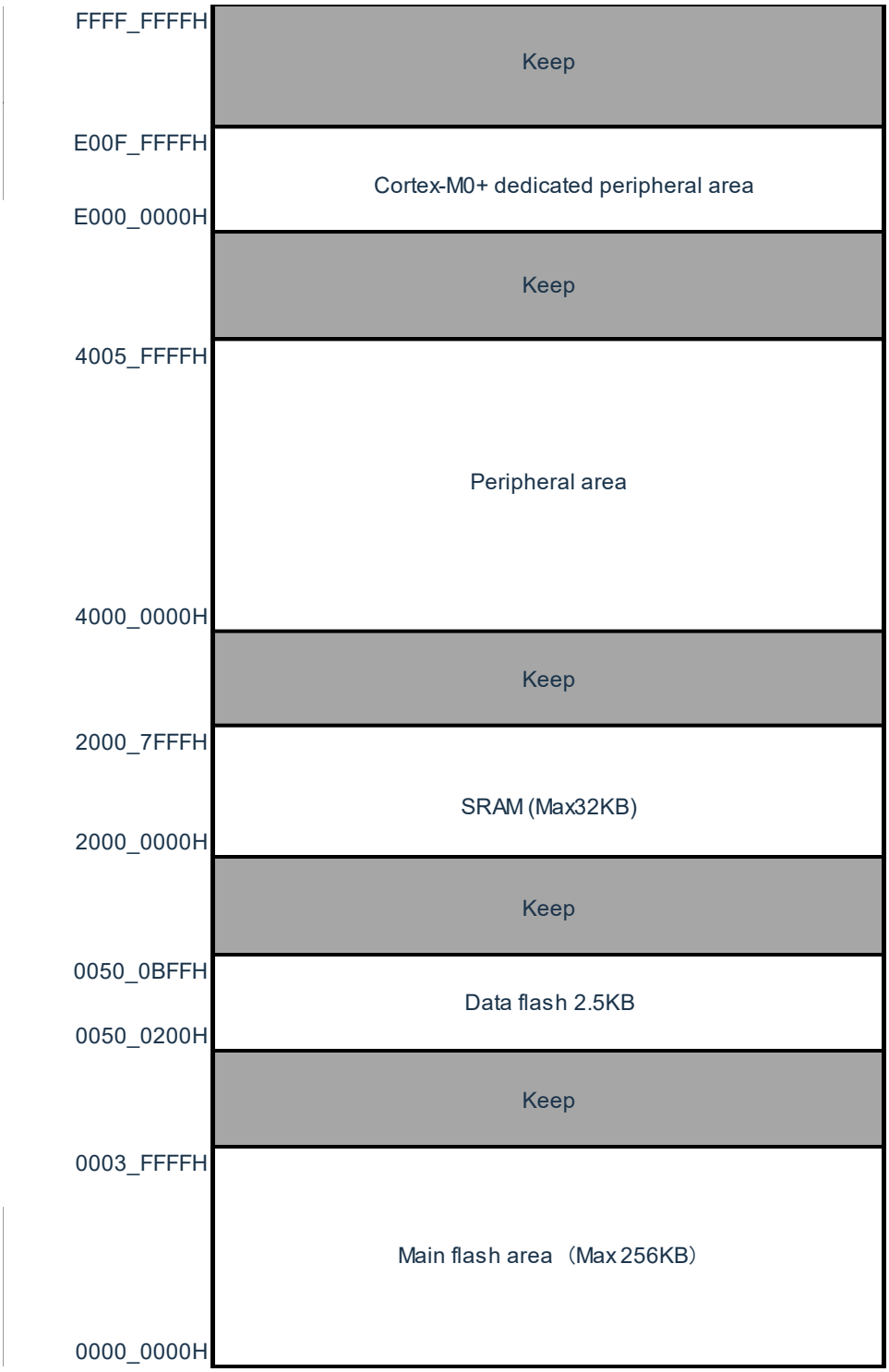
1) Make EVSS pin the same potential as VSS pin.
2) Make EVDD pin the same potential as VDD pin.
3) When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separateground lines.
4) Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

2 Block Diagram



Note: The above is for 80-pin product. Some functions of products below 80-pin are not supported.

3 Memory mapping



4 Pin function

4.1 Port function

The relationship between power supply and pins is as follows

80-pin, 64-pin product:

Power/ground	Corresponding pin
EVDD/EVSS	• Port pins other than P20～P27, P121～P124, P137 and RESETB
VDD/VSS	• P20～P27, P121～P124, P137 and RESETB

The 48-pin product uses a single power supply, and all pins are powered by VDD.

4.1.1 48-pin products

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Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/O	Analog function	ANI11/TXD1/VCIN10/TI00/TBCLK0/(TAO) /(INTP8)/CTxD0	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (VDD tolerance). P00 and P01 can be set to analog input
P01			ANI10/RXD1/VCIN11/TO00/TBCLK1 /TAIO/INTP10/CRxD0	
P10	I /O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI 8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13			TxD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14			RxD2/SDI20/SDA20/ TMIOB0/(TMIOC1)/ (SCLA0)/IrRxd	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)/CLK BUZ1	
P16			TI01/TO01/INTP5/TMIOC0/(RXD0)/(TMIO A1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(TXD 0) /(TMIOD0)	
P20	I /O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I /O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer.
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	

				Output of P30 can be set to N-ch Open-drain output (VDD tolerance).
P40	I /O	Input port	SWDIO	Port 4 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port
P41			(TAIO)	

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Function Name	I/O	After Reset Release	Alternate Function	Function
P50	I /O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO) /(TMIOC1)/(CRxD0)	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 can be set to TTL input buffer. Output of P50 and P51 can be set to N-ch opendrain output (VDD tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P60	I /O	Input port	SCLA0	Port 6 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60～P63 can be set to N-ch opendrain output (6V tolerance).
P61			SDAA0	
P62			SS00	
P63			—	
P70	I /O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 6-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch opendrain output (VDD tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21/(TXD1)	
P73			KR3/SDO01/(RXD1)	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P120	I /O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13. 1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by software, using internal pull-up resistors.
P136	I /O	Input port	INTP0	
P137			SWCLK	
P140	I /O	Input port	CLKBUZ0/INTP6	Port 14.

P146		Analog function	ANI15	3-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P146 and P147 can be set as analog input.
P147			ANI12/VREF0	
RESETB	I	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.

Note: Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Description of Alternate function,please refer to “4.2 pins other than port pins”.
Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.2 64-pin products

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Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/ O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (VDD tolerance). P00 and P02 to P04 can be set to analog input
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)	
P06			(INTP11)/(TAIO)	
P10	I/ O	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)/IrRxd	
P15			SCLK20/SCL20/TMIOD0/ (SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/ (RXD0) /(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(SDO00) /(TXD0)/(TMIOD0)	
P20	I/ O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I/ O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3. 2-bit I/O port.

P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch Open-drain output (VDD tolerance).

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Function Name	I/O	After Reset Release	Alternate Function	Function
P40	I/ O	Input port	SWDIO	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)	
P50	I/ O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO) /(TMIOC1)/(CRxD0)	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 andP51 can be set to TTL input buffer. Output of P50, p51 and P55 can be set to N-ch opendrain output (V_{DD} tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	I/ O	Input port	SCLA0	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60～P63 can be set to N-ch opendrain output (6V tolerance).
P61			SDAA0	
P62			SS00	
P63			—	
P70	I/ O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch opendrain output (EV_{DD} tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P120	I/ O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13.

P136	I/ O	Input port	INTP0	1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by software, using internal pull-up resistors.
P137			SWCLK	
P140	I/ O	Input port	CLKBUZ0/INTP6	Port 14. 4-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P146 and P147 can be set as analog input.
P141			CLKBUZ1/INTP7	
P146		Analog function	ANI15	
P147			ANI12/VREF0	
RESETB	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.。

Note: Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Description of Alternate function,please refer to “4.2 pins other than port pins”.
Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.3 80-pin products

(1/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/ O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00, P02 to P04 can be set to N-ch open-drain output (EV_{DD} tolerance). P02, P03 and P04 can be set to analog input
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)/TI17/TO17	
P06			(INTP11)/(TAIO)	
P10	I/ O	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EV_{DD} tolerance). P10 and P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)/IrRxd	
P15			SCLK20/SCL20/TMIOD0/ (SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0) /(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK0/(SDO00) /(TXD0)/(TMIOD0)	
P20	I/ O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I/ O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer.
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	

				Output of P30 can be set to N-ch Open-drain output (EV_{DD} tolerance).

(2/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P40	I/ O	Input port	SWDIO	Port 4 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P43 and P44 can be set to TTL input buffer. Output of P43 and P44 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)/SCLK31/SCL31	
P44			SDA31/SDI31	
P45			SDO31	
P50	I/ O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 and P55 can be set to TTL input buffer. Output of P50, P51 and P55 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	I/ O	Input port	SCLA0	Port 6 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 can be set to N-ch Open-drain output (6V tolerance).
P61			SDAA0	
P62			SS00/SCLA1	
P63			SDAA1	
P64			TI10/TO10/CTxD1	
P65			TI11/TO11/CRxD1	
P66			TI12/TO12	
P67			TI13/TO13	
P70	I/ O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch open-drain output (EV_{DD} tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P100	I/ O	Analog function	ANI16/TI14/TO14	Port 10. 1-bit I/O port. Input/output can be specified in 1-bit units.

				Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P110	I/ O	Input port	TI15/TO15	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P111			TI16/TO16	
P120	I/ O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13. 1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by software, using internal pull-up resistors.
P136	I/ O	Input port	INTP0	
P137			SWCLK	
P140	I/ O	Input port	CLKBUZ0/INTP6	Port 14. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P142 and P143 can be set to TTL input buffer. Output of P142, P143, and P144 can be set to N-ch open-drain output (EV_{DD} tolerance). P146 and P147 can be set to analog input
P141			CLKBUZ1/INTP7	
P142			SCLK30/SCL30	
P143			SDI30/RxD3/SDA30	
P144			SDO30/TxD3	
P146		Analog function	ANI15	
P147			ANI12/VREF0	
P150	I/ O	Analog function	ANI17	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to analog input
P151			ANI18	
P152			ANI19	
P153			ANI20	
RESETB	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).

Description of Alternate function,please refer to “4.2 pins other than port pins”.

Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register

4.2 Port multiplexing function

(1/2)

Function name	input/output	Function
ANI0 ～ANI20	input	Analog input of A/D converter
ANO0, ANO1	output	D/A converter output
INTP0 ～INTP11	input	External interrupt request input Designation of valid edges: rising edge, falling edge, rising and falling double edges
VCIN0	input	Analog voltage input of comparator 0
VCIN10, VCIN11, VCIN12, VCIN13	input	Comparator1's analog voltage/reference voltage input
VREF0	input	Reference voltage input of comparator0
VCOUT0, VCOUT1	output	Comparator output
PGA0IN，PGA1IN	input	PGA input
PGA0GND，PGA1GND	input	PGA reference input
KR0 ～KR7	input	Key interrupt input
CLKBUZ0, CLKBUZ1	output	Clock output / buzzer output
RTC1HZ	output	Real-time clock correction clock (1Hz) output
RESETB	input	Low-level active system reset input. When external reset is not used, it must be connected to V_{DD} directly or through a resistor.
CRxD0, CRxD1	input	CAN serial data input
CTxD0, CTxD1	output	CAN serial data output
RxD0 ～RxD3	input	Serial interface UART0, UART1, UART2 serial data input
TxD0 ～TxD3	output	Serial interface UART0, UART1, UART2 serial data output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31	output	Serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31 serial clock output
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31	input/ output	Serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31 serial clock input/ output
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21, SCLK30, SCLK31	input/ output	Serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31 serial clock input/ output
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21, SDI30, SDI31	input	Serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31 serial clock input/ output

(2/2)

Function name	input/output	Function
SS00	input	Chip select input of serial interface SSPI00
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21, SDO30, SDO31	output	Serial data output of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
SCLA0, SCLA1	input/ output	Serial interface IICA0, IICA1 clock input/output
SDAA0, SDAA1	input/ output	Serial interface IICA0, IICA1 serial data input/output
TI00～TI03	input	16-bit timer Timer4 external count clock/capture trigger input
TO00～TO03	output	Timer output of 16-bit timer Timer4
TI10～TI17	input	16-bit timer Timer8 external count clock/capture trigger input
TO10～TO17	output	Timer output of 16-bit timer Timer8
TAIO	input/ output	Timer TimerA input/output
TAO	output	TimerTimerA output
TMCLK	input	TimerTimerM external clock input
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	input/ output	Timer TimerM input/output
TBIO0, TBIO1	input/ output	Timer TimerB input/output
TBCLK0, TBCLK1	input	Timer TimerB external clock input
X1, X2	—	Connect the resonator for the main system clock.
EXCLK	input	External clock input of main system clock
XT1, XT2	—	Connect the resonator for the subsystem clock.
EXCLKS	input	External clock input for subsystem clock
VDD	—	＜48-pin product＞: Power supply for all pins ＜64, 80 pin product＞: Power supply for P20～P27, P121～P124, P137 and RESETB pins
EVDD	—	Power supply for port pins (except P20～P27, P121～P124, P137 and RESETB)
AVREFP	input	Positive (+) reference voltage input of A/D converter
AVREFM	input	Negative (–) reference voltage input of A/D converter
VSS	—	＜48-pin product＞: Ground potential of all pins ＜64, 80 pin product＞: Ground potential of P20～P27, P121～P124, P137 and RESETB pin
EVSS	—	Ground potential of port pins (except P20～P27, P121～P124, P137 and RESETB)
SWDIO	input/ output	SWD data interface
SWCLK	input	SWD clock interface

Remark: As a countermeasure for noise and locking, the bypass capacitor (about 0.1uF) must be connected with the shortest distance between VDD-VSS and EVDD-EVSS and thicker wiring.

5 Function summary

5.1 ARM® Cortex®-M0+ core

ARM's Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of a small pin count and low-power microcontroller, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and the expected high performance of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

The Cortex-M0(+) processor equipped with this product integrates the MPU memory protection unit: provides hardware management and protection of memory, and controls access rights. In addition, it also integrates the MTB on-chip tracking unit: users can experience better tracking and debugging, optimized exception capture mechanism, and can locate bugs more quickly.

BAT32G139 uses an embedded ARM core, so it is compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash

BAT32G139 has a built-in flash memory that can be programmed, erased and rewritten. Has the following functions:

- Programs and data share 256K storage space.
- 2.5KB dedicated data Flash memory
- Support page erasing, each page size is 512byte, erasing time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

5.2.2 SRAM

BAT32G139 has built-in 32K bytes of embedded SRAM.

5.3 Enhanced DMA controller

Built-in enhanced DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using CPU.

- It supports the start of DMA through peripheral function interrupts, and can realize real-time control through communication, timer and A/D.
- The transmission source/destination area is optional for the entire address space range (when the flash area is used as the destination address, the flash needs to be preset to the programming mode).
- Supports 4 transfer modes (normal transfer mode, repetitive transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage controller

The linkage controller links each peripheral function output event with the peripheral function trigger source. So as to realize the coordinated operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

The linkage controller has the following functions:

- The event signals can be linked together to realize the linkage of peripheral functions.
- 23 types of event input, 10 types of event trigger.

5.5 Clock generation and start

The clock generation circuit is a circuit that generates a clock for the CPU and peripheral hardware. There are the following 3 types of system clocks and clock oscillation circuits.

5.5.1 Main system clock

- X1 oscillator circuit: It can generate 1-20MHz clock oscillation by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): The frequency can be selected for oscillation by the option byte. After the reset is released, the CPU defaults to start running with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The highest frequency is 64Mhz, and the accuracy is ±1.0%.
- Input the external clock from the pin (X2): (1～20MHz), and the input of the external main system clock can be disabled by executing the deep sleep instruction or setting the MSTOP bit.

5.5.2 Subsystem clock

- XT1 oscillator circuit: It can generate 32.768kHz clock oscillation by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- Input the external clock from the pin (XT2): 32.768kHz, and the input of the external clock can be disabled by setting the XTSTOP bit.

5.5.3 Low-speed internal oscillator clock

- Low-speed internal oscillator (low-speed OCO): generates 15kHz (TYP.) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can be run by the low-speed internal oscillator clock:
- Watchdog timer (WWDT)
- Real Time Clock (RTC)
- 15-bit interval timer
- TimerA

5.5.4 PLL

- PLL: can be used as system clock. The source clock of the PLL can be either an external clock or an internal high-speed oscillator clock.

5.6 Power management

5.6.1 Power supply mode

VDD: external power supply, voltage range 1.8 to 5.5V
EVDD: external power supply, voltage range 1.8 to 5.5V
The voltage of the VDD pin must be equal to the voltage of the EVDD pin.

5.6.2 Power-on reset

The power-on reset circuit (POR) has the following functions:

- An internal reset signal is generated when the power is turned on. If the power supply voltage (VDD) is greater than the detection voltage (VPOR), the reset is released. However, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset.
- The power supply voltage (VDD) and the detection voltage (VPDR) are compared. When VDD<VPDR, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode before it falls below the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset. If you want to restart operation, you must confirm that the power supply voltage has returned to the operating voltage range.

5.6.3 Voltage detection

The voltage detection circuit sets the operation mode and detection voltage (VLVDH, VLVDL, VLVD) through the option byte. The voltage detection (LVD) circuit has the following functions:

- Compare the power supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD) and generate an internal reset or interrupt request signal.
- The detection voltage of the power supply voltage (VLVDH, VLVDL, VLVD) can select the detection level by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset. When the power supply drops, it must be transferred to the deep sleep mode before being lower than the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset.
- The operating voltage range varies according to the setting of the user option byte.

5.7 Low power consumption mode

BAT32G139 supports two low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing the sleep command. The sleep mode is a mode in which the CPU operating clock is stopped. Before setting the sleep mode, if the high-speed system clock oscillator circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode cannot reduce the operating current to the level of the deep sleep mode, it is an effective mode when you want to restart processing immediately through an interrupt request or when you want to perform intermittent operation frequently.
- Deep sleep mode: Enter the deep sleep mode by executing the deep sleep command. The deep sleep mode is a mode to stop the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stop the entire system. Can greatly reduce the operating current of the chip. Because the deep sleep mode can be cancelled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the wait time for stable oscillation when releasing the deep sleep mode, if you must start processing immediately with an interrupt request, you must select the sleep mode.

In either mode, the registers, flags, and data memory all retain the contents before the standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

5.8 Reset function

The following 7 methods to generate a reset signal:

1) Input external reset through RESETB pin.
2) Generate an internal reset through the program runaway detection of the watchdog timer.
3) The internal reset is generated by comparing the power supply voltage of the power-on reset (POR) circuit and the detection voltage.
4) The internal reset is generated by comparing the power supply voltage of the voltage detection circuit (LVD) and the detection voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset. After the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

5.9 Interrupt function

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor also supports multiple internal exceptions.

This product has processed 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI), and can support up to 96 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies from product to product.

		48-pin	64-pin	80-pin
Maskable interrupt	external	11	12	12
	internal	33	33	44

5.10 Real time clock (RTC)

The real-time clock (RTC) has the following functions.

- Counter with year, month, week, day, hour, minute and second.
- Fixed period interrupt function (period: 0.5 second, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm clock: week, hour, minute)
- 1Hz pin output function
- Support the division of the subsystem clock or the main system clock as the running clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up from deep sleep mode
- Support a wide range of clock correction functions

Only when the sub-system clock (32.768kHz) or the divided frequency of the main system clock is selected as the running clock of the RTC, the year, month, week, day, hour, minute and second can be counted. When the low-speed internal oscillator clock (15kHz) is selected, only the fixed cycle interrupt function can be used.

5.11 Watchdog timer

1 channel WWDT, 17bit watchdog timer is set to count operation by option byte. The watchdog timer runs on the low-speed internal oscillator clock (15kHz). The watchdog timer is used to detect program runaway. When a program out of control is detected, an internal reset signal is generated.

The following conditions are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the enable register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

5.12 SysTick timer

This timer is dedicated to the real-time operating system, but it can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-filling capacity counter reaches 0, a maskable system interrupt is generated.

5.13 Timer timer4

This product has built-in timer unit timer4 which contains 4 16-bit timers. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, please refer to the table below:

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Measurement of input pulse interval ● Measurement of the high/low level width of the input signal ● Delay counter	● One-shot pulse output ● PWM output ● Multiple PWM output

5.13.1 Independent channel operation function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer：Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output：Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter：Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Frequency divider function (only limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00), and then output from the output pin (TO00).
5) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
6) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.

7) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

5.13.2 Multi-channel linkage operation function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

5.13.3 8-bit timer operation function

The 8-bit timer operation function can use the 16-bit timer channel as a function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used)

5.13.4 LIN-bus support function

The timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: Start counting on the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a certain fixed value, it is considered as a wake-up signal.
2) Interval field detection: After detecting the wake-up signal, start counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the width of the low level is greater than or equal to a certain fixed value, it is regarded as an interval field.
3) Synchronous field pulse width measurement: After detecting the interval field, measure the low-level width and high-level width of the input signal of the UART serial data input pin (RxD). Calculate the baud rate based on the bit interval of the sync field measured in this way.

5.14 Timer timer8

The 80-pin product adds a built-in timer unit timer8 with 8 16-bit timers. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

5.14.1 Independent channel operation function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer：Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output：Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter：Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
5) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
6) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

5.14.2 Multi-channel linkage operation function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

5.14.3 8-bit timer operation function

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

5.15 TimerA

This product has a built-in 16bit timer timerA, which is composed of a reload register and a down counter. It can be used in the following working modes:

- Timer mode: count the counting source (the counting source can be a clock or an external event)
- Pulse output mode: count the counting source and output pulse when overflow
- Event counter mode: An external event is counted. Operation is possible in DEEPSLEEP mode.
- Pulse width measurement mode: An external pulse width is measured.
- Pulse period measurement mode: An external pulse period is measured.

5.16 TimerM

The product contains 2 channels of 16-bit timer timerM optimized for motor control. It has the following 4 working modes:

- Timer mode:
  - Input capture function (Transfer the counter value to a register with an external signal as the trigger)
  - Output compare function (Detect register value matches with a counter, and Pin output can be changed at detection)
  - PWM function (Output pulse of any width continuously)
- Reset synchronous PWM mode: Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode: Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode: Output PWM waveforms (2) with a fixed period

5.17 TimerB

TimerB is a 16-bit timer, supports the following three modes:

- Timer mode:
  - Input capture function: Count at the rising edge, falling edge, or both rising/falling edges
  - Output compare function: Low output/high output/toggle output
- PWM mode: PWM output available with any duty cycle
- Phase counting mode: Automatic measurement available for the counts of the two-phase encoder

5.18 TimerC

his product has a built-in 16bit timer timerC, which can be triggered by software, comparator or timer timerM to realize the input capture function.

5.19 15-bit interval timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at any time interval set in advance, and can be used to wake up from deep sleep mode.

5.20 Clock output/buzzer output control circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is realized by dedicated pins.

5.21 Universal serial communication unit

This product has 4 built-in universal serial communication units, and each unit has up to 4 serial communication channels. It can realize the communication functions of standard SPI, simple SPI, UART and simple I2C. Take the 80pin product as an example, the function allocation of each channel is as follows.

5.21.1 3-wire serial interface (simple SPI)

Synchronize data transmission and reception with the serial clock (SCK) output from the master control device.

This is a clock synchronous communication interface that uses 1 serial clock (SCK), 1 sending serial data (SO), and 1 receiving serial data (SI) to communicate with a total of 3 communication lines.

[data transmission and reception]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice

[clock control]

- Choice of master control or slave
- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Master communication: Max.fCLK/2

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.21.2 Simple SPI with slave chip select function

SPI serial communication interface supporting slave chip select input function. This is a clock synchronization that uses a slave chip select input (SSI), a serial clock (SCK), a sending serial data (SO), and a receiving serial data (SI) 4 communication lines for communication. Communication Interface.

[Data sending and receiving]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice
- Level setting of sending and receiving data

[clock control]

- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.21.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data reception (RxD). Use these two communication lines to send and receive data asynchronously (using the internal baud rate) with other communication parties according to the data frame (consisting of start bit, data, parity bit and stop bit). Full-duplex UART communication can be realized by using two channels dedicated for transmission (even-numbered channels) and dedicated for reception (odd-numbered channels), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data sending and receiving]

- 7-bit, 8-bit or 9-bit data length
- MSB/LSB priority choice
- Selection of level setting and reverse phase of sending and receiving data
- Additional parity check bit, parity check function
- Additional stop bit, stop bit detection

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

- Error interrupt caused by framing error, parity error or overflow error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Wake-up signal detection
- BF detection
- Measurement of synchronization field, calculation of baud rate

5.21.4 Simple I2C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I2C is designed for single communication with flash memory, A/D converters and other devices, it can only be used as a master device. The start condition and stop condition are the same as the operation control register, and must comply with the AC characteristics and be processed by software.

[Data sending and receiving]

- Main control sending, main control receiving (only limited to the main control function of single main control)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, use the upper 7 bits to specify the address, and use the lowest bit for R/W control)
- Generate start and stop conditions through software

[interrupt function]

- End of transmission interrupt

[Error detection flag]

- ACK error, overflow error

[Functions not supported by simple I2C]]

- Slave sending, slave receiving
- Multi-master control function (arbitration failure detection function)
- Waiting for detection function

5.22 Standard serial interface IICA

The serial interface IICA has the following 3 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I2C bus mode (supports multiple masters): This mode uses 2 lines of serial clock (SCLA) and serial data bus (SDAA) to transmit 8-bit data with multiple devices. In line with the I2C bus format, the master device can generate "start condition", "address", "indication of the transfer direction", "data" and "stop condition" for the slave device on the serial data bus. The slave device automatically detects the received status and data through hardware. This function can simplify the I2C bus control part of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain output, the serial clock line and the serial data bus require a pull-up resistor.
- Wake-up mode: In the deep sleep mode, when the extension code or the local station address from the autonomous control device is received, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). Set through the IICA control register.

5.23 Controller CAN

This product can support up to two general CAN bus interfaces.

5.24 Analog-to-digital converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog input to digital value and supports up to 21 channels of ADC analog input (ANI0～ANI20). The ADC contains the following functions:

- 12-bit resolution, conversion rate 1.42Msps.
- Trigger mode: support software trigger, hardware trigger and hardware trigger in standby state
- Channel selection: support two modes of single-channel selection and multi-channel scanning
- Conversion mode: support single conversion and continuous conversion
- Working voltage: Support the working voltage range of 1.8V≤VDD≤5.5V
- It can detect the built-in reference voltage (1.45V) and temperature sensor.

ADC can set various A/D conversion modes through the following mode combinations.

Trigger mode	Software trigger	Start the conversion by software operation.
	Hardware trigger no wait mode	Start the conversion by detecting the hardware trigger.
	Hardware trigger wait mode	In the conversion standby state with the power off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization wait time.
Channel selection mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Perform A/D conversion on 4 channels of analog input in sequence. It is possible to select 4 consecutive channels from ANI0 to ANI15 as analog input.
Conversion mode	Single conversion mode	Perform 1 A/D conversion on the selected channel.
	Continuous conversion mode	Perform continuous A/D conversion on the selected channel until it is stopped by software.
Sampling time/conversion time	Number of sampling clocks/number of conversion clocks	The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the Min value of the conversion clock is 31.5 clk.

5.25 Analog to digital conversion (DAC)

This product has a built-in 2-channel 8-bit resolution analog-to-digital converter DAC, which can convert digital input to analog signal. Has the following characteristics:

- 8-bit resolution D/A converter
- Support the output of two independent analog channels
- R-2R ladder method
- Built-in real-time output function

5.26 Programmable gain amplifier (PGA)

This product has two built-in programmable gain amplifiers (PGA0 and PGA1), which have the following functions:

- GAIN: X4, X8, X10, X12, X14, X16, X32
- The external pin (PGAGND) can be selected as the ground of the negative feedback resistance of the PGA (can be used as a differential mode)
- The output of PGA0 can be selected as analog input for A/D converter or analog input for positive terminal of comparator0 (CMP0).
- PGA1 output can be selected as analog input for A/D converter

5.27 Comparator (CMP)

This product has built-in two channels with hysteresis comparatorCMP0 and CMP1, with the following functions:

- The external input and reference multi-channels of CMP1 are optional.
- Can select external reference voltage input and internal reference voltage for reference voltage.
- The elimination width of the noise elimination digital filter can be selected.
- Can detect the valid edge of the comparator output and generate an interrupt signal.
- It can detect the valid edge of the comparator output and output the event signal to the linkage controller.

5.28 Two-wire serial debug port (SW-DP)

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

5.29 Security function

5.29.1 Flash CRC calculation function (high-speed CRC, general-purpose CRC)

Detect the data error of flash memory through CRC operation.

According to different purposes and conditions of use, the following 2 CRCs can be used respectively.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash area at high speed。
- General CRC: In CPU operation, it is not limited to the code flash area but can be used for multi-purpose checking.

5.29.2 RAM Parity error detection function

When reading RAM data, detect parity errors.

5.29.3 SFR protection function

Prevent the important SFR (Special Function Register) from being rewritten due to CPU runaway.

5.29.4 Illegal memory access detection function

Detect illegal access to illegal memory area (area without memory or area with restricted access).

5.29.5 Frequency detection function

Can use timer4 unit to self-check CPU or peripheral hardware clock frequency.

5.29.6 A/D test function

Perform A/D conversion on the A/D converter's positive (+) reference voltage, negative (–) reference voltage, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage Self-test.

5.29.7 Digital output signal level detection function of input/ output port

When the input/output port is in output mode, the output level of the pin can be read.

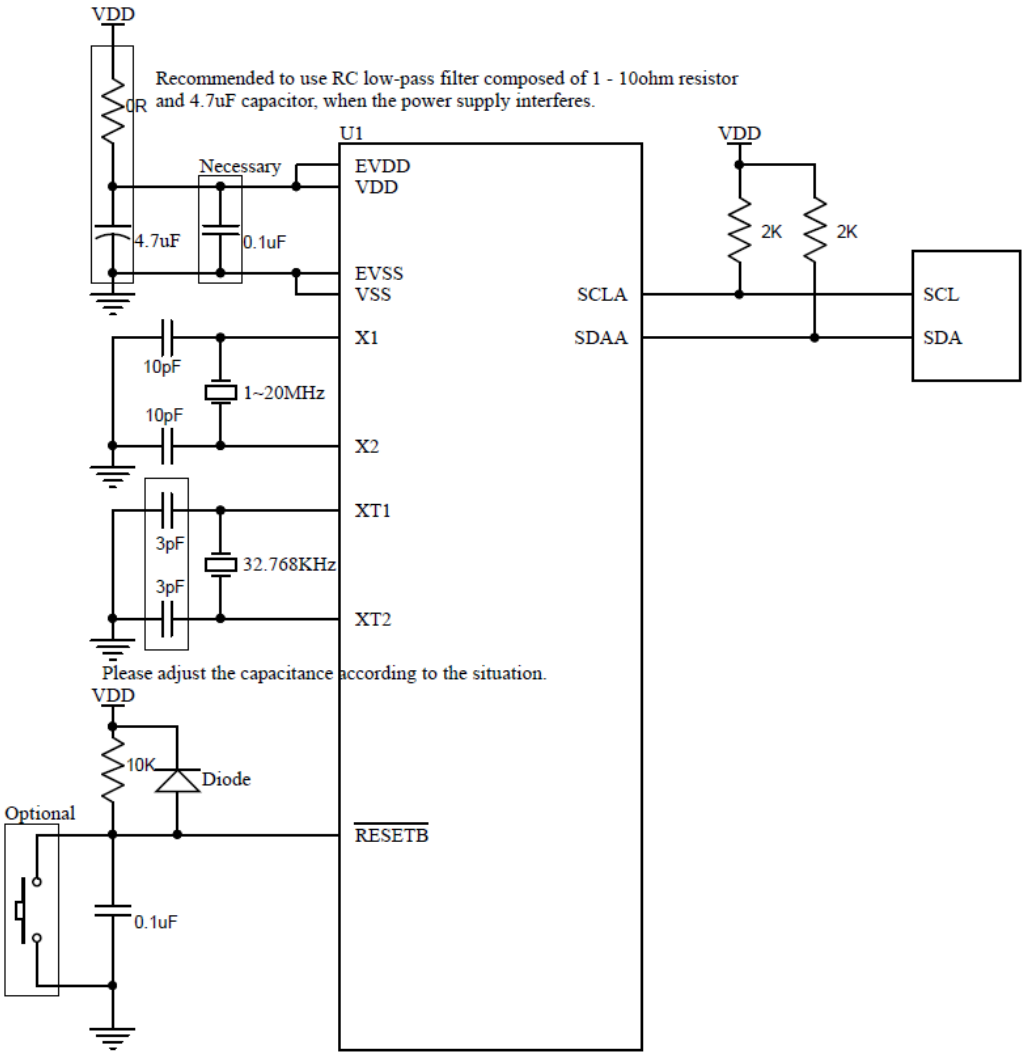
5.30 Key function

The input pin (KR0～KR7) can be interrupted by the key to generate a key interrupt (INTKR).

6 Electrical characteristics

6.1 Typical application peripheral circuit

The device connection reference of the typical MCU application peripheral circuit is as follows:



6.2 Absolute maximum voltage rating

(TA=–40～+105℃)

Item	Symbol	Condition	Rating	Unit
Source voltage	VDD		－0.5～+6.5	V
	EVDD		－0.5～+6.5	V
Input voltage	VI1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P136, P140～P144, P146～P147, P150～P153	－0.3～EVDD+0.3 and －0.3～VDD+0.3 note1	V
	VI2	P60～P63(N-channel open drain)	－0.3～+6.5	V
	VI3	P20～P27, P121～P124, P137, EXCLK, EXCLKS, RESETB	－0.3～VDD+0.3 note1	V
Output voltage	VO1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P136, P140～P144, P146～P147, P150～P153	－0.3～EVDD+0.3 and －0.3～VDD+0.3 note1	V
	VO2	P20～P27, P137	－0.3～VDD+0.3 note1	V
Analog input voltage	VAI1	ANI8～ANI20	－0.3～EVDD+0.3 and －0.3～AVREF(+)+0.3 note1, 2	V
	VAI2	ANI0～ANI7	－0.3～VDD+0.3 and －0.3～AVREF(+)+0.3 note1, 2	V

Note：1. Do not exceed 6.5V.

2. The pin of the A/D conversion target cannot exceed AVREF(+)+0.3.

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remarks：

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. AVREF(+): The positive (+) reference voltage of the A/D converter
3. Use VSS as the reference voltage.

6.3 Absolute maximum current rating

(TA=–40～+105℃)

Item	Symbol	Condition		Rating	Unit
High level output current	IOH1	Each pin	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153	－40	mA
		Total pins －170mA	P00～P04, P40～P45, P120, P130, P136, P137, P140～P144, P150～P153	－70	mA
			P05, P06, P10～P17, P30, P31, P50～P55, P64～P67, P70～P77, P100, P110～P111, P146, P147	－100	mA
	IOH2	Each pin	P20～P27	－3	mA
		Total pins		－15	mA
Low-level output current	IOL1	Each pin	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153	40	mA
		Total pins 170mA	P00～P04, P40～P45, P120, P130, P136, P137, P140～P144, P150～P153	100	mA
			P05, P06, P10～P17, P30, P31, P50～P55, P60～P67, P70～P77, P100, P110～P111, P146, P147	120	mA
	IOL2	Total pins	P20～P27	15	mA
		Total pins		45	mA
Working temperature	TA	Normally run		－40～+105	℃
		When flash programming			
Storage temperature	Tstg			－65～+150	℃

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.4 Oscillation circuit characteristics

6.4.1 X1, XT1 characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	Resonator	condition	MIN	TYP	MAX	unit
X1 clock oscillation frequency (fx)	Ceramic resonator/ crystal resonator	1.8V≤VDD≤5.5V	1.0	-	20.0	MHz
XT1 clock oscillation frequency (fxt)	Crystal resonator	1.8V≤VDD≤5.5V	32	32.768	35	kHz

Note：

1. It only indicates the allowable frequency range of the oscillation circuit. Please refer to the AC characteristics for the command execution time.
2. Please entrust the resonator manufacturer to evaluate after installing the circuit, and use it after confirming the oscillation characteristics.

6.4.2 Internal oscillator characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Resonator	Condition	MIN	TYP	MAX	unit
High-speed internal oscillator clock frequency (fIH)note1,2		1.0		64.0	MHz
Clock frequency accuracy of high-speed internal oscillator	TA= - 20～+105℃	-1.0		+1.0	%
	TA= - 40～ - 20℃	-1.5		+1.5	%
Clock frequency of low-speed internal oscillator (fIL)		10	15	20	kHz

Note：

1. Select the frequency of the high-speed internal oscillator by the option byte.
2. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.

6.4.3 PLL oscillator characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Resonator	Condition	MIN	TYP	MAX	unit
PLL input frequency note1		4.0		8.0	MHz
PLL lock time		40			μs

Note：1. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.

6.5 DC characteristics

6.5.1 Pin characteristics

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High leveloutput Current note1	IOH1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153 1 pin alone	1.8V≤EVDD≤5.5V –40～+85℃			-12.0 note2	mA
			1.8V≤EVDD≤5.5V 85～+105℃			-6.0 note2	
		P00～P04, P40～P45, P120, P130, P136, P137, P140～P144, P150～P153 Total pins (when duty cycle ≤70% note3)	4.0V≤EVDD≤5.5V –40～+85℃			-60.0	mA
			4.0V≤EVDD≤5.5V 85～+105℃			-30.0	
			2.4V≤EVDD＜4.0V			-12.0	mA
			1.8V≤EVDD＜2.4V			-6.0	mA
		P05, P06, P10～P17, P30, P31, P50～P55, P64～P67, P70～P77, P100, P110～P111, P146, P147 Total pins (when duty cycle ≤70% note3)	4.0V≤EVDD≤5.5V –40～+85℃			-80.0	mA
			4.0V≤EVDD≤5.5V 85～+105℃			-30.0	
			2.4V≤EVDD＜4.0V			-20.0	mA
			1.8V≤EVDD＜2.4V			-10.0	mA
		Total pins (when duty cycle ≤70% note3)	1.8V≤EVDD≤5.5V –40～+85℃			-140.0	mA
			1.8V≤EVDD≤5.5V 85～+105℃			-60.0	
	IOH2	P20 ～ P27 1 pin alone	1.8V≤VDD≤5.5V			-2.5 note2	mA
		Total pins (when duty cycle ≤70% note3)	1.8V≤VDD≤5.5V			-10	mA

Note：

1. This is the current value that guarantees the operation of the device even if current flows from the EVDD, VDD pin to the output pin.

2. Can not exceed the total current value.

3. This is the output current value of "duty cycle≤70%condition".

To change the output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%).

• The total output current of the pins = (IOH×0.7)/(n×0.01)

＜example＞ IOH =–10.0mA, n =80%

The total output current of the pins = (–10.0×0.7)/(80×0.01) ≈ –8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Note: In the N-channel open-drain mode, the pin set to the N-channel open-drain valid does not output a high

level.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

item	symbol	condition		MIN	TYP	MAX	unit
Low-level output current[note 1]	IOL1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153 1 pin alone	1.8V≤EVDD≤5.5V –40～+85℃			35[note2]	mA
			1.8V≤EVDD≤5.5V 85～+105℃			20 [note2]	
		P00～P04, P40～P45, P120, P130, P136, P137, P140～P144, P150～P153 Total pins (when duty cycle ≤70%[note3])	4.0V≤EVDD≤5.5V –40～+85℃			100	mA
			4.0V≤EVDD≤5.5V 85～+105℃			70	
			2.4V≤EVDD＜4.0V			30	mA
			1.8V≤EVDD＜2.4V			15	mA
		P05, P06, P10～P17, P30, P31, P50～P55, P60～P67, P70～P77, P100, P110～P111, P146, P147 Total pins (when duty cycle ≤70%[note3])	4.0V≤EVDD≤5.5V –40～+85℃			120	mA
			4.0V≤EVDD≤5.5V 85～+105℃			80	
			2.4V≤EVDD＜4.0V			40	mA
			1.8V≤EVDD＜2.4V			20	mA
		Total pins (when duty cycle ≤70%[note3])	1.8V≤EVDD≤5.5V –40～+85℃			150	mA
			1.8V≤EVDD≤5.5V 85～+105℃			100	
	IOL2	P20～P271 pin alone	1.8V≤VDD≤5.5V			10[note2]	mA
		Total pins (when duty cycle ≤70%[note3])	1.8V≤VDD≤5.5V			40	mA

Note:

1. This is the current value that guarantees the operation of the device even if current flows from the output pin to the EVSS and VSS pins.

2. Can not exceed the total current value.

3. This is the output current value of "duty cycle≤70% condition"。

The output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%)

• The total output current of the pins = (IOL×0.7)/(n×0.01)

＜example＞ IOL= 10.0mA, n = 80%

The total output current of the pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High level input voltage	VIH1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P136, P140～P144, P146～P147, P150～P153	Schmidt input	0.8EVDD		EVDD	V
	VIH2	P01, P03, P04, P10, P14～P17, P30, P43～P44, P50, P55, P142～P143	TTL input 4.0V≤EVDD≤5.5V	2.2		EVDD	V
			TTL input 3.3V≤EVDD<4.0V	2.0		EVDD	V
			TTL input 1.8V≤EVDD<3.3V	1.5		EVDD	V
	VIH3	P20～P27, P137		0.7VDD		VDD	V
	VIH4	P60～P63		0.7EVDD		6.0	V
	VIH5	P121～P124, EXCLK, EXCLKS, RESETB		0.8VDD		VDD	V
Low-level input voltage	VIL1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P136, P140～P144, P146～P147, P150～P153	Schmidt input	0		0.2EVDD	V
	VIL2	P01, P03, P04, P10, P14～P17, P30, P43～P44, P50, P55, P142～P143	TTL input 4.0V≤EVDD≤5.5V	0		0.8	V
			TTL input 3.3V≤EVDD<4.0V	0		0.5	V
			TTL input 1.8V≤EVDD<3.3V	0		0.32	V
	VIL3	P20～P27, P137		0		0.3VDD	V
	VIL4	P60～P63		0		0.3EVDD	V
	VIL5	P121～P124, EXCLK, EXCLKS, RESETB		0		0.2VDD	V

Note: Even in the N-channel open-drain mode, the maximum VIH (MAX.) of the pin that is set to the N-channel open-drain is also EVDD.

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40 ～ +105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High level output voltage	VOH1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153	4.0V≤EVDD≤5.5V, IOH1= - 12.0mA	EVDD - 1.5			V
			4.0V≤EVDD≤5.5V, IOH1= - 6.0mA	EVDD - 0.7			V
			2.4V≤EVDD≤5.5V, IOH1= - 3.0mA	EVDD - 0.6			V
			1.8V≤EVDD≤5.5V, IOH1= - 2mA	EVDD - 0.5			V
	VOH2	P20～P27	4.0V≤VDD≤5.5V, IOH2= - 2.5mA	EVDD - 1.5			V
			4.0V≤VDD≤5.5V, IOH2= - 1.5mA	EVDD - 0.7			V
			2.4V≤VDD≤5.5V, IOH2= - 0.5mA	EVDD - 0.6			V
			1.8V≤VDD≤5.5V, IOH2= - 0.4mA	VDD - 0.5			V
Low-level output voltage	VOL1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P130, P136, P137, P140～P144, P146～P147, P150～P153	4.0V≤EVDD≤5.5V, IOL1=35.0mA			1.2	V
			4.0V≤EVDD≤5.5V, IOL1=20.0mA			0.7	V
			2.4V≤EVDD≤5.5V, IOL1=9.0mA			0.4	V
			1.8V≤EVDD≤5.5V, IOL1=6.0mA			0.4	V
	VOL2	P20～P27	4.0V≤VDD≤5.5V, IOL2=10.0mA			1.2	V
			4.0V≤VDD≤5.5V, IOL2=6.0mA			0.7	V
			2.4V≤VDD≤5.5V, IOL2=2.5mA			0.4	V
			1.8V≤VDD≤5.5V, IOL2=2.0mA			0.4	V

Note: In the N-channel open-drain mode, the pin set to the N-channel open-drain valid does not output a high level.

Remarks: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High-level input leakage current	ILIH1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P130, P136, P140～P144, P146～P147, P150～P153	VI=EVDD			1	μA
	ILIH2	P20～P27, P137, RESETB	VI=VDD			1	μA
	ILIH3	P121～P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VDD, when input port and external clock input			1	μA
			VI=VDD, when the resonator is connected			10	μA
Low-level input leakage current	ILIL1	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P60～P67, P70～P77, P100, P110～P111, P120, P130, P136, P140～P144, P146～P147, P150～P153	VI=EVSS			-1	μA
	ILIL2	P20～P27, P137, RESETB	VI=VSS			-1	μA
	ILIL3	P121～P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VSS, when input port and external clock input			-1	μA
			VI=VSS, when the resonator is connected			-10	μA
Internal pull-up resistor	RU	P00～P06, P10～P17, P30, P31, P40～P45, P50～P55, P64～P67, P70～P77, P100, P110～P111, P120, P136, P137, P140～P144, P146～P147	VI=EVSS, when input port	10	30	100	kΩ

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.5.2 Power supply current characteristics

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition				MIN.	TYP.	MAX.	unit
current note1	IDD1	Operating mode	High-speed internal oscillator	fHOCO=64MHz, fIH=64MHz note3			7.6	12	mA
				fHOCO=48MHz, fIH=48MHz note3			7.0	10	
				fHOCO=32MHz, fIH=32MHz note3			6.0	7.8	
			High-speed main system clock	fMX=20MHz note2	Input square wave		4.0	5.2	mA
					Connect the crystal		4.0	5.2	
			Subsystem clock operation	fSUB=32.768kHz note4	Input square wave		70	85	uA
					Connect the crystal		70	85	
	IDD2	Sleep mode	High-speed internal oscillator	fHOCO=64MHz, fIH=64MHz note3			2.0	6.8	mA
				fHOCO=48MHz, fIH=48MHz note3			1.6	5.0	
				fHOCO=32MHz, fIH=32MHz note3			1.2	3.5	
			High-speed main system clock	fMX=20MHz note2	Input square wave		0.7	2.2	mA
					Connect the crystal		0.7	2.2	
			Subsystem clock operation	fSUB=32.768kHz note5	Input square wave		1.2	14.5	uA
					Connect the crystal		1.2	14.5	
	IDD3 note 6	Deep sleep mode note7	TA=–40℃~+70℃ VDD=3.0V				0.8	4.0	uA
			TA=–40℃~+85℃ VDD=3.0V				0.8	7.0	
			TA=–40℃~+105℃ VDD=3.0V				0.8	14.5	

Note:

1) Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD or VSS, EVSS. The values of the TYP. column include the current of the CPU executing the multiplication instruction (IDD1),not including the peripheral operation current. The values below the MAX. column include the current of the CPU executing the multiplication instruction (IDD1) and the peripheral operation current.However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
2) This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.
3) This is the case where the high-speed main system clock and subsystem clock stop oscillating.
4) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating.
5) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains the current flowing to the RTC, but does not include the 15-bit interval timer and watchdog timer current
6) Does not include current to RTC, 15-bit interval timer and watchdog timer.
7) For the current value when the subsystem clock is running in the deep sleep mode, please refer to the current value when the subsystem clock is running in the sleep mode.

Note:

1) f_{HOCO}: The clock frequency of the high-speed internal oscillator, fIH: the system clock frequency provided by the high-speed internal oscillator.
2) f_{SUB} ： External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3) f_{MX}: External main system clock frequency (X1/X2 clock oscillation frequency).
4) TYP. The temperature condition of the value is TA=25°C.

(T_A=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V)

parameter	symbol	condition		MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator operating current	IFIL note1				0.2		uA
RTC operating current	IRTC note1,2,3				0.04		uA
15-bit interval timer operating current	IIT note 1,2,4				0.02		uA
Watchdog timer operating current	IWDT note 1,2,5	fIL=15kHz			0.22		uA
A/D converter operating current	IADC note 1,6	ADC HS mode @64MHz			2.2		mA
		ADC HS mode @4MHz			1.3		mA
		ADC LC mode @24MHz			1.1		mA
		ADC LC mode @4MHz			0.8		mA
D/A converter operating current	IDAC note 1,8	Each channel			1.4		mA
PGA operating current		Each channel			480	700	uA
comparator operating current	ICMP note 1,9	Each channel	Does not use internal reference voltage		60	100	uA
			Use internal reference voltage		80	140	uA
LVD operating current	ILVD note 1,7				0.08		uA

注:

1) This is the current flowing through VDD.
2) This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating。
3) This is the current that only flows to the real-time clock (RTC) (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the real-time clock is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IRTC. In addition, when low-speed internal oscillator is selected, IFIL must be added. IDD2 when the subsystem clock is running contains the operating current of the real-time clock.
4) This is the current that only flows to the 15-bit interval timer (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the 15-bit interval timer is running in run mode or sleep mode, the current value of the microcontroller is the value of IDD1 or IDD2 plus IIT. In addition, when low-speed internal oscillator is selected, IFIL must be added.
5) This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). When the watchdog timer is running, the current value of the microcontroller is IDD1 or IDD2 or IDD3 plus the value of IWDT.
6) This is the current that only flows to the A/D converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IADC.
7) This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ILVD.

8) This is the current that only flows to the D/A converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IADC.

9) This is the current that only flows to the comparator circuit. When the comparator circuit is running, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ICMP.

Note: 1. f_{IL} : Clock frequency of low-speed internal oscillator.

2. TYP. The temperature condition of the value is T_A=25℃.

6.6 AC characteristic

(T_A=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
Instruction cycle (Minimum instruction execution time)	TCY	The main system clock (fMAIN) runs	1.8V≤VDD≤5.5V	0.015625		1	μs
		Subsystem clock (fSUB) operation	1.8V≤VDD≤5.5V	28.5	30.5	31.3	μs
External system clock frequency	fEX	1.8V≤VDD≤5.5V		1.0		20.0	MHz
	fEXS	1.8V≤VDD≤5.5V		32.0		35.0	kHz
High and low level width of external system clock input	tEXH, tEXL	1.8V≤VDD≤5.5V		24			ns
	tEXHS, tEXLS	1.8V≤VDD≤5.5V		13.7			μs
TI00 ～ TI03, TI10 ～ TI17 output frequency	tTIH, tTIL	1.8V≤VDD≤5.5V		1/fMCK+10			ns
Input period of timer timerA	tC	TAIO	2.4V≤EVDD≤5.5V	100			ns
			1.8V≤EVDD＜2.4V	300			ns
The high and low level width of timerA input	tTAIH, tTAIL	TAIO	2.4V≤EVDD≤5.5V	40			ns
			1.8V≤EVDD＜2.4V	120			ns

Note: f_{MCK}: timer4, timer8 operating clock frequency of timer4 unit

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS =0V)

item	symbol	condition		MIN	TYP	MAX	unit
Timer M input high and low level width	tTMIH, tTMIL	TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/fCLK			ns
Timer M forced cut-off signal input low-level width	tTMSIL	P136/INTP0	2MHz＜fCLK≤48MHz	1			μs
			fCLK ≤ 2MHz	1/fCLK+1			μs
Timer B input high and low level width	tTBIH, tTBIL	TBIOA, TBIOB		2.5/fCLK			ns
TO00 ～ TO03, TO10 ～ TO17, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB Output frequency	fTO	4.0V≤EVDD≤5.5V				16	MHz
		2.4V≤EVDD＜4.0V				8	MHz
		1.8V≤EVDD＜2.4V				4	MHz
CLKBUZ0, CLKBUZ1 Output frequency	fPCL	4.0V≤EVDD≤5.5V				16	MHz
		2.4V≤EVDD＜4.0V				8	MHz
		1.8V≤EVDD＜2.4V				4	MHz
High and low level width of interrupt input	tINTH, tINTL	INTP0 ～ INTP11	1.8V≤EVDD≤5.5V	1			μs
High and low level width of key interrupt input	tKR	KR0 ～ KR7	1.8V≤EVDD≤5.5V	250			ns
RESETB low-level width	tRSL			10			μs

6.7 Peripheral features

6.7.1 Universal interface unit

1) UART mode

(TA=–40～+85℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	condition		Specification Value		unit
			MIN	MAX	
Transfer rate	1.8V ≤ EVDD ≤ 5.5V			fMCK/6	bps
		The theoretical value of the maximum transfer rate fMCK=fCLK		10.6	Mbps

(TA=+85～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	condition		Specification Value		unit
			MIN	MAX	
Transfer rate	1.8V ≤ EVDD ≤ 5.5V			fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		5.3	Mbps

2) Three-wire SPImode (master mode, internal clock output)

(TA=–40～+105℃, 1.8V ⩽ EVDD = VDD ⩽ 5.5V, VSS=EVSS=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY1	tKCY1 ≥ 2/fCLK	4.0V ≤ EVDD ≤ 5.5V	31.25		62.5		ns
			2.7V ≤ EVDD ≤ 5.5V	41.67		83.33		
			2.4V ≤ EVDD ≤ 5.5V	65		125		ns
			1.8V ≤ EVDD ≤ 5.5V	125		250		ns
SCLKp high/low level width	tKH1, tKL1	4.0V ≤ EVDD ≤ 5.5V		tKCY1/2–4		tKCY1/2–7		ns
		2.7V ≤ EVDD ≤ 5.5V		tKCY1/2–5		tKCY1/2–10		ns
		2.4V ≤ EVDD ≤ 5.5V		tKCY1/2–10		tKCY1/2–20		ns
		1.8V ≤ EVDD ≤ 5.5V		tKCY1/2–19		tKCY1/2–38		ns
SDIp preparation time (to SCLKp↑)	tSIK1	4.0V ≤ EVDD ≤ 5.5V		12		23		ns
		2.7V ≤ EVDD ≤ 5.5V		17		33		ns
		2.4V ≤ EVDD ≤ 5.5V		20		38		ns
		1.8V ≤ EVDD ≤ 5.5V		28		55		ns
SDIp hold time (to SCLKp↑)	tKSI1	1.8V ≤ EVDD ≤ 5.5V		5		10		ns
SCLKp↓→SDOp output delay time	tKSO1	1.8V ≤ EVDD ≤ 5.5V C=20pF note1			5		10	ns

note1.：C is the load capacitance of the SCLKp and SDOp output lines。

Note: Through the port inputmode register and the port outputmode register, the SDIp pin is selected as the normal input buffer and theSDOp the pin and SCLKp pin are selected as the usual output mode.

3) Three-wire SPImode (slave mode, external clock input)

(T_A=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY2	4.0V ≤ EVDD ≤ 5.5V	20MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤20MHz	6/fMCK		12/fMCK		ns
		2.7V ≤ EVDD ≤ 5.5V	16MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤16MHz	6/fMCK		12/fMCK		ns
		2.4V ≤ EVDD ≤ 5.5V		6/fMCK and 500		12/fMCK and 1000		ns
		1.8V ≤ EVDD ≤ 5.5V		6/fMCK and 750		12/fMCK and 1500		ns
SCLKp high/low level width	tKH2, tKL2	4.0V ≤ EVDD ≤ 5.5V		tKCY1/2–7		tKCY1/2–14		ns
		2.7V ≤ EVDD ≤ 5.5V		tKCY1/2–8		tKCY1/2–16		ns
		1.8V ≤ EVDD ≤ 5.5V		tKCY1/2–18		tKCY1/2–36		ns
SDIp preparation time (to SCLKp↑)	tSIK2	2.7V ≤ EVDD ≤ 5.5V		1/fMCK+20		1/fMCK+40		ns
		1.8V ≤ EVDD ≤ 5.5V		1/fMCK+30		1/fMCK+60		ns
SDIp hold time (to SCLKp↑)	tKSI2	1.8V ≤ EVDD ≤ 5.5V		1/fMCK+31		1/fMCK+62		ns
SCLKp↓→SDOp output delay time	tKSO2	2.7V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK+44		2/fMCK+66	ns
		2.4V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK+75		2/fMCK+113	ns
		1.8V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK+100		2/fMCK+150	ns

note1：C is the load capacitance of the SCLKp and SDOp output lines.

Note: Through the port inputmode register and the port outputmode register, The SDIp pin and SCLKp pin are selected as the normal input buffer and the SDOp pin is selected as the normal output mode.

4) Four-wire SPI mode (slave mode, external clock input)

(T_A= –40～+105℃, 1.8V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SSI00 set up time	tSSIK	DAPmn=0	2.7V ≤ EVDD ≤ 5.5V	120		240		ns
			1.8V ≤ EVDD ≤ 5.5V	200		400		ns
		DAPmn=1	2.7V ≤ EVDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤ EVDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ EVDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤ EVDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
		DAPmn=1	2.7V ≤ EVDD ≤ 5.5V	120		240		ns
			1.8V ≤ EVDD ≤ 5.5V	200		400		ns

Note: Through the port inputmode register and the port outputmode register, The SDIp pin and SCLKp pin are selected as the normal input buffer and the SDOp pin is selected as the normal output mode.

5) Simple IIC mode

(T_A=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V)

item	symbol	condition	–40 ～ +85℃		+85 ～ +105℃		unit
			MIN	MAX	MIN	MAX	
SCLr Clock frequency	fSCL	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		1000 note1		400nite1	kHz
		1.8V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		400 note1		100note1	kHz
		1.8V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		300 note1		75note1	kHz
Hold time when SCLr is low	tLOW	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Hold time when SCLr is high	tHIGH	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Data establishment time (received)	tSU:DAT	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK+85 note 2		1/fMCK+220 note 2		ns
		1.8V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1/fMCK+145 note 2		1/fMCK+580 note 2		ns
		1.8V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1/fMCK+230 note 2		1/fMCK+1200 note 2		ns
Data retention time (send)	tHD:DAT	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		305		770	ns
		1.8V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		355		1420	ns
		1.8V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		405		2070	ns

Note: 1. Must be set to at least fMCK/4.

2. The set value of fMCK cannot exceed the holding time of SCLr= “L” and SCLr= “H”.

6.7.2 Serial interface IICA

1) I2C standard mode

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLAr clock frequency	fSCL	Standard mode: fCLK≥1MHz		100	kHz
Start condition set up time	tSU: STA		4.7		μs
Start condition hold time note1	tHD: STA		4.0		μs
Hold time when SCLAr is low	tLOW		4.7		μs
Hold time when SCLAr is high	tHIGH		4.0		μs
Data establishment time (received)	tSU:DAT		250		ns
Data retention time (send)note2	tHD:DAT		0	3.45	μs
Stop condition set up time	tSU: STO		4.0		μs
Bus idle time	tBUF		4.7		μs

note：

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note：

The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I2C fast mode

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLAr clock frequency	fSCL	Fast mode: fCLK≥3.5MHz		400	kHz
Start condition set up time	tSU: STA		0.6		μs
Start condition hold time note1	tHD: STA		0.6		μs
Hold when SCLAr is low time	tLOW		1.3		μs
Hold when SCLAr is high time	tHIGH		0.6		μs
Data set up time (received)	tSU: DAT		100		ns
Data hold time (send)note2	tHD: DAT		0	0.9	μs
Stop condition set up time	tSU: STO		0.6		μs
Bus idle time	tBUF		1.3		μs

Note:

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK)。

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Fast mode: Cb=320pF, Rb=1.1kΩ

3) I2C enhanced fast mode

(TA=–40～+105°C, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLAr clock frequency	fSCL	Enhanced fast mode: fCLK≥10MHz		1000	kHz
Start condition set up time	tSU: STA		0.26		μs
Start condition hold time note1	tHD: STA		0.26		μs
Hold time when SCLAr is low	tLOW		0.5		μs
When SCLAr is high hold time	tHIGH		0.26		μs
Data set up time (received)	tSU: DAT		50		ns
Data hold time (send)note2	tHD: DAT		0	0.45	μs
Stop condition set up time	tSU: STO		0.26		μs
Bus idle time	tBUF		0.5		μs

note：

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1kΩ

6.8 Analog characteristic

6.8.1 A/D converter characteristic

The distinction of A/D converter characteristic

Reference voltage / Input channel	Reference voltage (+) =AVREFP Reference voltage (--) =AVREFM	Reference voltage (+) =VDD Reference voltage (--) =VSS
ANI0～ANI20	See 6.8.1(1)。	See 6.8.1 (2)。
Internal reference voltage, output voltage of temperature sensor		

1) Select the case of reference voltage (+)=AV_{REFP}/ANI0, reference voltage (–)=AV_{REFM}/ANI1

(TA=-40～+105℃, 1.8V≤AVREFP≤EVDD=VDD≤5.5V, VSS=0V, reference voltage (+)=AVREFP, reference voltage (–)=AVREFM=0V)

item	symbol	condition		MIN.		TYP.	MAX.	unit
Resolution	RES					12		bit
Composite error note1	AINL	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V			3		LSB
Conversion time note3	t_{CONV}	12-bit resolution Conversion target: ANI2～ANI15	1.8V≤VDD≤5.5V	45				Tmclk
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	1.8V≤VDD≤5.5V	72				Tmclk
Zero error note1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V			0		LSB
Full scale error note1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V			0		LSB
Integral linearity error note1	ILE	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V				±1	LSB
Differential linearity error note1	DLE	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2～ANI20		0			AV_{REFP}	V
		Internal reference voltage (1.8V≤VDD≤5.5V)			V_{BGR} note2			V
		The output voltage of the temperature sensor (1.8V≤VDD≤5.5V)			V_{TMPS25} note2			V

Note: 1. Does not include quantization error (±1/2 LSB).

2. Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage"。

3. Tmclk is the AD action clock cycle, the maximum action frequency is 48MHz.

2) Select the case of reference voltage (+)=V_{DD} and reference voltage (-)=V_{SS}

(T_A=–40～+105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V, reference voltage (+) =V_{DD}, reference voltage (–)=V_{SS})

item	symbol	condition		MIN.	TYP.	MAX.	unit
Resolution	RES				12		bit
Composite error note 1	AINL	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		6		LSB
Conversion time note 3	t_{CONV}	12-bit resolution Conversion target: ANI0～ANI15	1.8V≤VDD≤5.5V	45			Tmclk
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	1.8V≤VDD≤5.5V	72			Tmclk
Zero error note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Full scale error note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Integral linearity error note 1	ILE	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V			±2	LSB
Differential linearity error note 1	DLE	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V			±3	LSB
Analog input voltage	V_{AIN}	ANI0～ANI7		0		V_{DD}	V
		ANI8～ANI20		0		EV_{DD}	V
		Internal reference voltage (1.8V≤VDD≤5.5V)		V_{BGR} note2			V
		The output voltage of the temperature sensor (1.8V≤VDD≤5.5V)		V_{TMPS25} note2			V

Note: 1. Does not include quantization error (±1/2 LSB).

2. Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage".

3. Tmclk is the AD action clock cycle, the maximum action frequency is 64MHz.

6.8.2 Characteristic of temperature sensor/internal reference voltage

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition	MIN	TYP	MAX	unit
The output voltage of the temperature sensor	VTMPS25	TA=25℃		1.09		V
Internal reference voltage	VBGR	TA=–40～105℃	1.38	1.45	1.5	V
Temperature Coefficient	FVTMPS			-3.5		mV/℃
Stable operation waiting time	tAMP		5			μs

6.8.3 D/A converter

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition		MIN.	TYP.	MAX.	unit
Resolution	RES					8	bit
Composite error	AINL	Rload=4MΩ	1.8V≤VDD≤5.5V			±2.5	LSB
		Rload=8MΩ	1.8V≤VDD≤5.5V			±2.5	LSB
stable schedule	tSET	Cload=20pF	2.7V ≤ VDD ≤ 5.5V			3	μs
			1.8V ≤ VDD < 2.7V			6	μs

6.8.4 comparator

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
input deviation voltage	V_{IOCMP}				±10	±40	mV
input voltage range	Ivcmp			0		VDD	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register: 7FH ~ 80H (m = 0, 1)				±2	LSB
		others				±1	LSB
Response time	tCR, tCF	input amplitude ±100mV			70	150	ns
Stable operation time$_{note1}$	tCMP	CMPn=0->1	VDD= 3.3 ~ 5.5V			1	μs
			VDD= 1.8 ~ 3.3V			3	
Reference voltage stabilization time	tVR	CVRE=0->1 note2				20	μs
operating current	I_{CMPDD}	Separately, it is defined as the operation current of peripheral functions.					

note1: The time required from the enable of the comparator action (CMPnEN=0 —>1) to meeting the various DC/AC style requirements of CMP.

note2: After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled after the reference voltage stabilization time (CnOE bit = 1; n = 0 to 1)

6.8.5 Programmable gain amplifier PGA

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

symbol	parameter	condition		MIN.	TYP.	MAX.	Unit
Input deviation voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9xVDD/Gain	V
Output voltage range	V_{IOHPGA}			0.93xVDD			V
	V_{IOLPGA}					0.07xVDD	V
Gain deviation		x4				±1	%
		x8				±1	%
		x10				±1	%
		x12				±2	%
		x14				±2	%
		x16				±2	%
		x32				±3	%
Conversion rate	SR_{RPGA}	rise Vin= 0.1VDD/gain to 0.9VDD/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			V/us
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			1.8 V ≤ VDD ≤ 4.0V	0.5			
	SR_{FPGA}	drop Vin= 0.1VDD/gain to 0.9VDD/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			1.8 V ≤ VDD ≤ 4.0V	0.5			
Stable operation time Note 1	t_{PGA}	x4				5	us
		x8				5	us
		x10				5	us
		x12				10	us
		x14				10	us
		x16				10	us
		x32				10	us
Working current	I_{PGADD}	Separately, it is defined as the operation current of peripheral functions.					

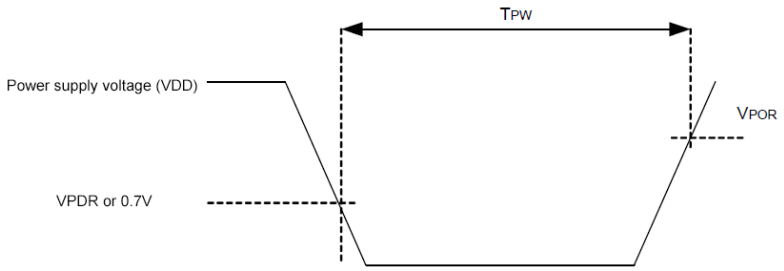
Note1: The time required from PGA action enable (PGAEN=1) to meeting various DC and AC style requirements of PGA.

6.8.6 POR circuit characteristic

(T_A=–40～+105℃, V_{SS}=0V)

item	symbol	condition	MIN	TYP	MAX	unit
Detection voltage	VPOR	When the power supply voltage rises		1.60	1.75	V
	VPDR	When the power supply voltage drops	1.37	1.50	1.55	V
Minimum pulse width[note1]	TPW		300			μs

note1: This is the time required for POR to reset when VDD is lower than VPDR. In addition, in the deep sleep mode, when the main system clock (fMAIN) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC), the oscillation of the main system clock (fMAIN) is stopped from VDD lower than 0.7V to rise above VPOR. Time required for POR reset.



6.8.7 LVD circuit characteristic

1) Reset mode and interrupt mode

(T_A=–40～+105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

item	symbol	condition	MIN	TYP	MAX	unit
Detection voltage	VLVD0	power supply voltage rises		4.06		V
		power supply voltage drops		3.98		V
	VLVD1	power supply voltage rises		3.75		V
		power supply voltage drops		3.67		V
	VLVD2	power supply voltage rises		3.13		V
		power supply voltage drops		3.06		V
	VLVD3	power supply voltage rises		3.02		V
		power supply voltage drops		2.96		V
	VLVD4	power supply voltage rises		2.92		V
		power supply voltage drops		2.86		V
	VLVD5	power supply voltage rises		2.81		V
		power supply voltage drops		2.75		V
	VLVD6	power supply voltage rises		2.71		V
		power supply voltage drops		2.65		V
	VLVD7	power supply voltage rises		2.61		V
		power supply voltage drops		2.55		V
	VLVD8	power supply voltage rises		2.50		V
		power supply voltage drops		2.45		V
	VLVD9	power supply voltage rises		2.09		V
		power supply voltage drops		2.04		V
	VLVD10	power supply voltage rises		1.98		V
		power supply voltage drops		1.94		V
	VLVD11	power supply voltage rises		1.88		V
		power supply voltage drops		1.84		V
Minimum pulse width	tLW		300			μs
Detection delay					300	μs

2) Interrupt and reset mode

(T_A=–40～+105℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V)

item	symbo	condition		MIN.	TYP.	MAX.	unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 0, 0, Decrease reset voltage			1.63		V
	V_{LVDA1}	LVIS1, LVIS0=1, 0	rising reset release voltage		1.77		V
			drop interrupt voltage		1.73		V
	V_{LVDA2}	LVIS1, LVIS0=0, 1	rising reset release voltage		1.88		V
			drop interrupt voltage		1.84		V
	V_{LVDA3}	LVIS1, LVIS0=0, 0	rising reset release voltage		2.92		V
			drop interrupt voltage		2.86		V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 0, 1, decrease reset voltage			1.84		V
	V_{LVDB1}	LVIS1, LVIS0=1, 0	rising reset release voltage		1.98		V
			drop interrupt voltage		1.94		V
	V_{LVDB2}	LVIS1, LVIS0=0, 1	rising reset release voltage		2.09		V
			drop interrupt voltage		2.04		V
	V_{LVDB3}	LVIS1, LVIS0=0, 0	rising reset release voltage		3.13		V
			drop interrupt voltage		3.06		V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 0, decrease reset voltage			2.45		V
	V_{LVDC1}	LVIS1, LVIS0=1, 0	rising reset release voltage		2.61		V
			drop interrupt voltage		2.55		V
	V_{LVDC2}	LVIS1, LVIS0=0, 1	rising reset release voltage		2.71		V
			drop interrupt voltage		2.65		V
	V_{LVDC3}	LVIS1, LVIS0=0, 0	rising reset release voltage		3.75		V
			drop interrupt voltage		3.67		V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 1, decrease reset voltage			2.75		V
	V_{LVDD1}	LVIS1, LVIS0=1, 0	rising reset release voltage		2.92		V
			drop interrupt voltage		2.86		V
	V_{LVDD2}	LVIS1, LVIS0=0, 1	rising reset release voltage		3.02		V
			drop interrupt voltage		2.96		V
	V_{LVDD3}	LVIS1, LVIS0=0, 0	rising reset release voltage		4.06		V
			drop interrupt voltage		3.98		V

6.8.8 The rising slope of the power supply voltage characteristic

(T_A=–40～+105℃, V_{SS}=0V)

item	symbol	condition	MIN	TYP	MAX	unit
The rising slope of the power supply voltage	SVDD				54	V/ms

6.9 Memory characteristic

6.9.1 Flash Memory characteristic

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
Tprog	Word Program(32bit)	Ta=–40～+105℃	24	30	μs
Terase	Sector erase(512B)	Ta=–40～+105℃	4	5	ms
	Chip erase	Ta=–40～+105℃	20	40	ms
NEND	Endurance	Ta=–40～+105℃	100		kcycle
tRET	Data retention	100 kcycle(note2) at Ta = 105℃	20		Years

Note1: Data based on characterization results, not tested in production.

Note2: Cycling performed over the whole temperature range.

6.9.2 RAM Memory characteristic

(TA=–40～+105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=EVSS=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
$V_{ramhold}$	RAM Hold Voltage	Ta=–40～+105℃	0.8		V

6.10 Electrical sensitivity characteristic

6.10.1 Electrostatic discharge (ESD) characteristic

Symbol	Parameter	Conditions	Class	Passed Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA = +25℃, conforming to JESD22-A114	3A	6000	V

Note: Data based on characterization results, not tested in production.

6.10.2 Static latch-up(LU) characteristic

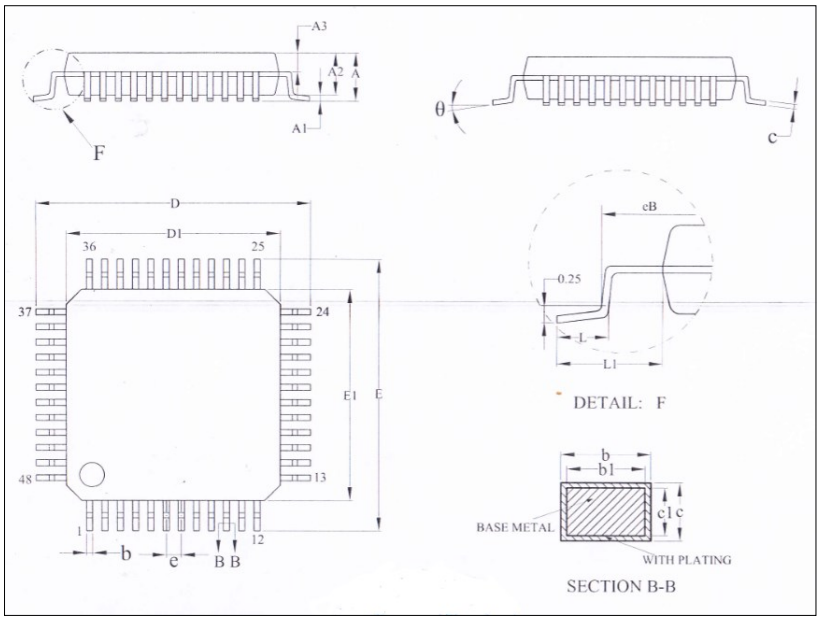
Symbol	Parameter	Conditions	Class
LU	Static latch-up class	TA = +25℃ conforming to JESD78E	I LevelA

Note: Data based on characterization results, not tested in production.

7 Package size chart

7.1 48-pin product

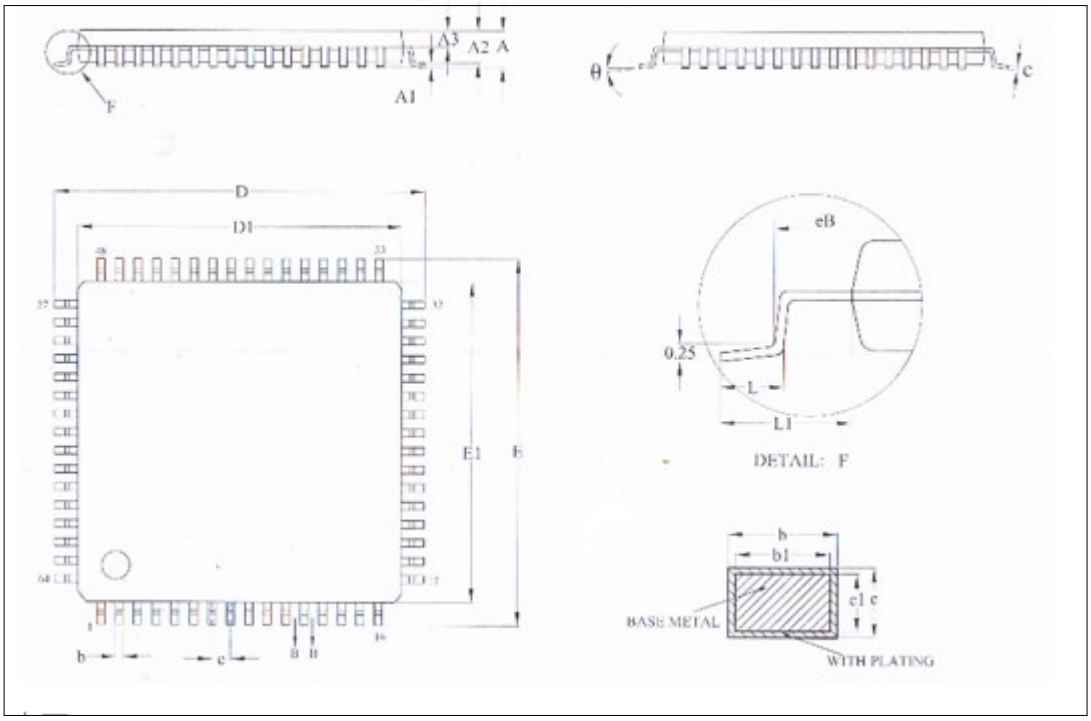
48LQFP (7x7mm, 0.5mm spacing)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

7.2 64-pin product

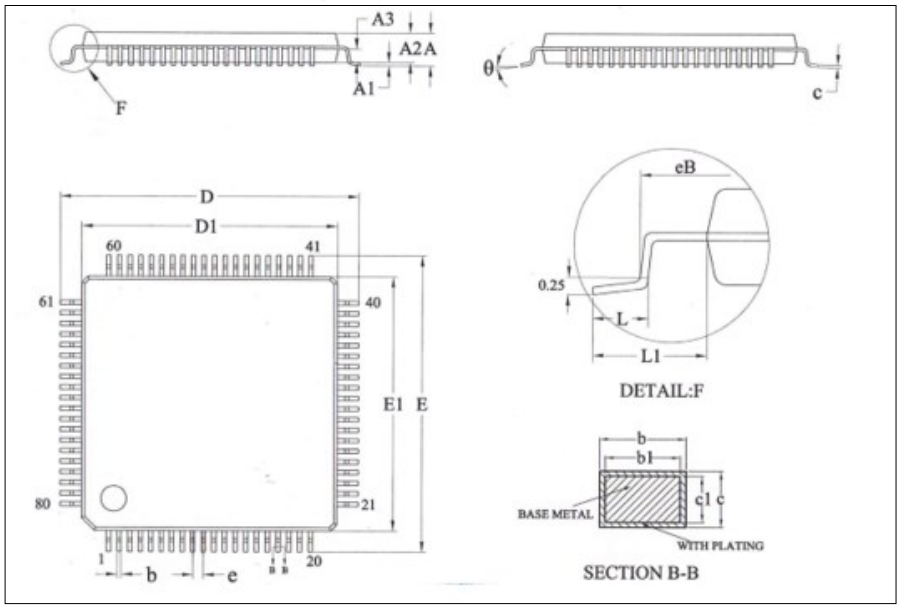
64LQFP (7x7mm, 0.4mm spacing)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

7.3 80-pin product

80LQFP (12×12mm, 0.5mm spacing)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	7°

8 Revision History

Revision	Date	Modify content	
		Page/section	content
1.0	2021.01.11	—	Initial verison
1.1	2021.07.20	6.10	Update the electrical sensitivity characteristic data
1.2	2021.08.24	6.4.3	Fix some mistakes
1.3	2022.01.24	P2	Fix some mistakes